» Kontron User's Guide «

KTH81/mITX

KTQ87/mITX

KTH81/Flex

KTQ87/Flex

KTD-N0882-L

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Document Revision History

Revision	Date	By	Comment
L	Sept 13th 2017	CW	Note to warn about carefully connecting the power connector
K	Jan. 12th 2017	CW	System Memory Support corrected
J	April 2016	GSZ	NEW Memory SKU
I	March 5th 2015	MLA	I7-4790S, I5-4590S added. EXT_BAT max. 3.47 V. Always On jumper description corrected.
H	July 16th 2014	MLA	Top text correction. Improved cooler information. Feature connector corrections. BIOS part upgraded.
G	May 27th 2014	MLA	Display configuration table improved. BIOS part added.
F	Feb. 26th 2014	MLA	Mating connector list updated. Pentium data added. Added KTH81/Flex and KTQ87/Flex. Updated document layout.
E	Sep. 23rd 2013	JS MLA	CPU table updated, Graphics data, FAN3 & 4 not supported. Audio Connector description correction. KTH81 included. Connector list updated.
D	July 3rd 2013	JS	Audio section update, page 30. CPU table updated. Picture update.
C	May 24th 2013	JS	Entire document revised
B	May 24th 2013	JS	Section 2.5 revised
A	May 15th 2013	JS	Feature port revised (FAN3/4 not supported)
0	April 14th 2013	JS	Preliminary version

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- CPU Board
  1. Type.
  2. Part Number (find PN on label)
  3. Serial Number if available (find SN on label)
- Configuration
  1. DRAM Type and Size.
  2. BIOS Revision (find the version info in the BIOS Setup).
  3. BIOS Settings different than *Default* Settings (refer to the BIOS Setup section).
- System
  1. O/S Make and Version.
  2. Driver Version numbers (Graphics, Network, and Audio).
  3. Attached Hardware: Harddisks, CD-Rom, LCD Panels etc.

If the Kontron Technology product seems to be defect and you want to return it for repair, please follow the guide lines from the following page:

http://kontron.com/services/rma-information/kontron-technology-a-s/

1 Introduction

This manual describes the KTH81/mITX, KTQ87/mITX, KTH81/Flex & KTQ87/Flex boards made by KONTRON Technology A/S. The boards will also be denoted KTQ87 & KTH81.

The KTQ87/KTH81 boards are based on the Q87/H81 chipsets supporting 4rd generation Intel® Haswell i7 -, i5 2Core and 4Core desktop processors, Haswell Dual Core Pentium and Haswell Dual Core Celeron. See "Processor Support Table" for more specific details.

The differences between the four types of boards are listed in this table:

Feature	KTH81/mITX	KTQ87/mITX	KTH81/Flex	KTQ87/Flex
Form factor	mITX	mITX	Flex ATX	Flex ATX
PCIex16	Gen2	Gen3	Gen2	Gen3
Vpro	-	Depends on CPU	-	Depends on CPU
AMT	-	Yes	-	Yes
RAID	-	Yes	-	Yes
DP	2x (DP0, DP1)	3x (DP0, DP1,DP2)	2x (DP0, DP1)	3x (DP0, DP1,DP2)
LVDS	-	-	Yes (=> no DP1)	Yes (=> no DP1)
USB	2x USB3.0/2.0 8x USB2.0	4x USB3.0/2.0 6x USB2.0	2x USB3.0/2.0 8x USB2.0	4x USB3.0/2.0 8x USB2.0
LPC	-	-	2x10 pin row	2x10 pin row
DIMM slots	2x	2x	2x	4x
PCIe slots	PCIex16, Gen2. mPCIe (w. USB)	PCIex16, Gen3 mPCIe (w. USB)	PCIex16, Gen2 PCIex2 (x16 slot) + PCIex1	PCIex16, Gen3 PCIex4 (x16 slot) + PCIex1
mSATA	1x (w. USB, LPC)	1x (w. USB,LPC)	-	-
SATA	1x Gen3 2x Gen2	5x, Gen3	2x Gen3 2x Gen2	6x, Gen3
PCI Slot	-	-	1x	1x
Kbd/Mse	-	-	6-pin row	6-pin row
Fan connectors	CPU, Sys	CPU, Sys	CPU, Sys1, Sys2	CPU, Sys1, Sys2

Use of this Users Guide implies a basic knowledge of PC-AT hard- and software. This manual is focused on describing the KTQ87 / KTH81 board's special features and is not intended to be a standard PC-AT textbook.

New users are recommended to study the short installation procedure stated in the following chapter before switching-on the power.

All configuration and setup of the CPU board is either done automatically or manually by the user via the BIOS setup menus. Only exceptions are the "Clear CMOS" Jumper and the "Always On" jumper.

Latest revision of this manual, datasheet, BIOS, drivers, BSP's (Board Support Packages), Mechanical drawings (2D and 3D) can be downloaded from here: http://www.kontron.com/products/boards-and-mezzanines/embedded-motherboards/

2 Installation Procedure

2.1 Installing the Board

To get the board running follow these steps. If the board shipped from KONTRON has already components like RAM and CPU cooler mounted, then relevant steps below can be skipped.

1. **Turn off the PSU (Power Supply Unit)**

Warning: Turn off PSU (Power Supply Unit) completely (no mains power connected to the PSU) or leave the Power Connectors unconnected while configuring the board. Otherwise components (RAM, LAN cards etc.) might get damaged. Make sure only to use standard ATX PSU. Running the board with non-compliant ATX PSU may damage the board within minutes.

2. **Insert the DDR3 DIMM 240pin DIMM module(s)**
   Be careful to push it in the slot(s) before locking the tabs. For a list of approved DDR3 DIMMs contact your Distributor or FAE. See also chapter “System Memory Support”.

3. **Install the processor**
   The CPU is keyed and will only mount in the CPU socket in one way. Use finger to open/ close the CPU socket. Refer to supported processor overview for details.

4. **Cooler Installation**
   Make sure the heat paste etc. on the cooler is intact and cover the full area of the CPU. Connect Cooler Fan electrically to the FAN_CPU connector.

5. **Connecting Interfaces**
   Insert all external cables for hard disk, keyboard etc. A monitor must be connected in order to change BIOS settings.

6. **Connect and turn on PSU**
   Connect PSU to the board by the ATXPWR (24pole power plug) and the ATX4p (4-pole power plug).

Warning: When connecting and disconnecting the power connector to the board, handle with care to prevent bending the PCB board. Bending the PCB board may damage components and can result in malfunction or prevent the board from functioning.

7. **Power Button**
   If the board does not start by itself when switching on the ATX PSU AC mains, then follow these instructions to start the board. Install the Always On Jumper in the Always On position or toggle the PWRBTN_IN# signal (available in the FRONTPNL connector), by momentary shorting pins 16 (PWRBTN_IN#) and pin 18 (GND). A “normally open” switch is recommended.

8. **BIOS Setup**
   Enter the BIOS setup by pressing the <F2> key during boot up.
   Enter “Exit Menu” and Load Setup Defaults.
   Refer to the “BIOS Configuration / Setup“ section of this manual for details on BIOS setup.

Note: To clear all BIOS settings, including Password protection, activate "Load Default BIOS Settings" Jumper for ≈10 sec (without power connected).

9. Mounting the board in chassis

Warning: When mounting the board to chassis etc. please notice that the board contains components on both sides of the PCB which can easily be damaged if board is handled without reasonable care. A damaged component can result in malfunction or no function at all.

When fixing the Motherboard on a chassis it is recommended using screws with integrated washer and a diameter of ≈7mm. Do not use washers with teeth, as they can damage the PCB and cause short circuits.

2.2 Requirements IEC60950

Take care when designing chassis interface connectors in order to fulfil the IEC60950 standard.

When an interface or connector has a VCC (or other power) pin which is directly connected to a power plane like the VCC plane:
To protect the external power lines of the peripheral devices the customer has to ensure:

- Wires have suitable rating to withstand the maximum available power.
- That the enclosure of the peripheral device fulfils the fire protecting requirements of IEC60950.

Lithium battery precautions

CAUTION! Danger of explosion if battery is incorrectly re- placed. Replace only with same or equivalent type recommended by manufacturer. Dispose of used batteries according to the manufacturer's instruc- tions.	**VORSICHT!** Explosionsgefahr bei unsachgemäßem Austausch der Batterie. Ersatz nur durch den selben oder einen vom Hersteller empfohlenen gleichwertigen Typ. Entsorgung gebrauchter Batterien nach Anga- ben des Herstellers.
ATTENTION! Risque d'explosion avec l'échange inadéquat de la batterie. Remplacement seulement par le même ou un type équivalent recommandé par le producteur. L'évacuation des batteries usagées conformément à des indications du fabricant.	**PRECAUCION!** Peligro de explosión si la batería se sustituye incorrectamente. Sustituya solamente por el mismo o tipo equivalente recomendado por el fabricante. Disponga las baterías usadas según las instrucciones del fabricante.
ADVARSEL! Lithiumbatteri – Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.	**ADVARSEL!** Eksplosjonsfare ved feilaktig skifte av batteri. Benytt samme batteritype eller en tilsvarende type anbefalt av apparatfabrikanten. Brukte batterier kasseres i henhold til fabrikantens instruksjoner.
VARNING! Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.	**VAROITUS!** Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan lalteval- mistajan suosittelemaan tyyppiln. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

3 System Specifications

3.1 Component Main Data

The table below summarizes the features of the KTH81/mITX, KTQ87/mITX, KTH81/Flex and KTQ87/Flex.

Form factor	mITX (miniITX) 170,18 mm by 170,18 mm Flex (Flex-ATX) 190,5 mm by 228,6 mm
Processor	Support the following 4rd Generation Intel® Core™ (Haswell Desktop) processors via LGA1150 H3 Socket (max 65W TDP) • Intel® Core™ i7 • Intel® Core™ i5 • Intel® Core™ i3 • Intel® Pentium • Intel® Celeron (4x 5 GT/s point-to-point DMI interface to PCH and 2/3/4/6/8MB internal cache).
Chipset	Intel Q87 PCH (Platform Controller Hub) • Intel ® VT-d (Virtualisation Technology for Directed I/O) • Intel ® TXT (Trusted Execution Technology) • Intel ® vPRO • Intel ® AMT (Active Management Technology) version 9.0 • Intel ® AT (Anti-Theft Technology) • Intel ® HD Audio Technology • Intel ® RST (Rapid Storage Technology) • Intel ® RRT (Rapid Recover Technology) • SATA (Serial ATA) 6Gb/s and 3Gb/s. • USB revision 2.0 • USB revision 3.0 • PCI Express revision 2.0 • ACPI 3.0b compliant • Triple Display support (Triple Graphic Pipes) • Blue-ray HD video playback Intel H81 PCH (Platform Controller Hub) • Intel ® VT-d (Virtualisation Technology for Directed I/O) • Intel ® TXT (Trusted Execution Technology) • Intel ® Rapid storage technology: ACHI Only • Intel ® HD Audio Technology • SATA (Serial ATA) 6Gb/s and 3Gb/s. • USB revision 2.0 • USB revision 3.0 • PCI Express revision 2.0 • ACPI 3.0b compliant • Dual Display support (Two Graphic Pipes) • Blue-ray HD video playback

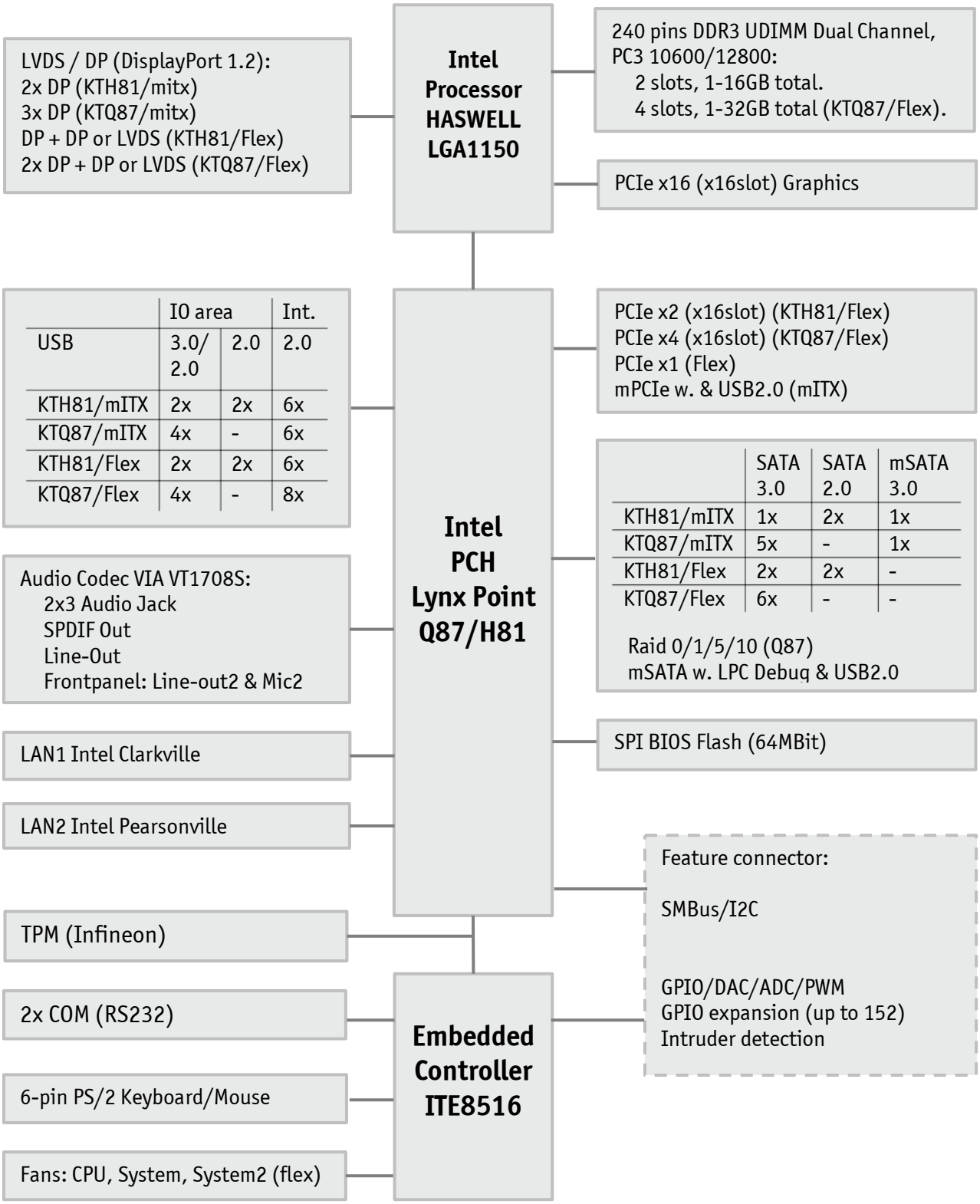
Security	Intel® Integrated TPM 1.2 support
Memory	• DDR3 DIMM 240pin socket (2/4 sockets on mITX/Flex) • Support single and dual ranks DDR3 1333/1600MT/s (PC3-10600/PC3-12800) • Support system memory from 1x 1GB up to 2x/4x 8GB on mITX/Flex. Notes: Less than 4GB displayed in System Properties using 32bit OS (Shared Video Memory/PCI resources is subtracted) • ECC not supported (PGA processors do not support ECC)
Management	Intel® Active Management Technology (Intel® AMT) 9.0 (KTQ87 only)
Audio	Audio, 7.1 Channel High Definition Audio Codec using the VIA VT1708S codec • Line-in • Headphone stereo signals. • Surround output: SIDE, LFE, CEN, BACK and FRONT • Microphone: MIC1 and MIC2 • SPDIF-Out (electrical Interface only) • On-board speaker (Electromagnetic Sound Generator like Hycom HY-05LF)
Video	Intel ® i5 & i7 4rd Generation Desktop processors support Intel ® HD Graphics 4600. 2 or 3x digital display ports via the Intel® Haswell CPU. • 2x DP (DisplayPorts), comply with DisplayPort 1.2 specification. (H81 only) • 3x DP (DisplayPorts), comply with DisplayPort 1.2 specification. (Q87 only) • HDMI panel support via DP to HDMI Adapter Converter. • DVI panel support via DP to DVI Adapter Converter. • VGA panel support via DP to VGA Adapter Converter. • LVDS panel JEIDA/VESA up to 2x24 bit (Flex only) • Triple independent pipes (Q87 only) • Triple independent or cloned displays are supported from OS. • Any 3 or 2 displays via DP0, DP1, DP2 (Q87 only) or LVDS (Flex only) can be used. (DP1 and LVDS cannot both be active at the same time).
Peripheral interfaces	• 4x USB3.0 / USB2.0 on I/O area (Q87 only) • 2x USB3.0 / USB2.0 plus 2x USB2.0 on I/O area (H81 only) • 4x USB2.0 ports on internal pinrows (KTQM87/mITX, KTHM81/mITX, KTHM81/Flex) • 6x USB2.0 ports on internal pinrows (KTQM87/Flex) • 1x USB2.0 ports on internal mPCIe connector (mITX only) • 1x USB2.0 ports on internal mSATA connector (mITX only) • 2x Serial ports (RS232) on internal pinrows • 1x SATA3.0, 2x SATA2.0 and 1x mSATA (SATA3.0, USB, LPC) (KTH81/mITX) • 5x SATA3.0 and 1x mSATA (SATA3.0, USB, LPC) (KTQ87/mITX) • 2x SATA3.0 and 2x SATA2.0 (KTH81/Flex) • 6x SATA3.0 (KTQ87/Flex) • RAID 0/1/5/10 support (Q87 only)

LAN Support	• 1x 10/100/1000Mbits/s LAN (ETHER1): Intel® Clarksville WGI218-LM Gigabit PHY w. AMT 9.0 (Q87 only) Intel® Clarksville WGI218-V Gigabit PHY (H81 only) • 1x 10/100/1000Mbits/s LAN (ETHER2) Intel® Pearsonville I211AT • PXE Netboot supported. • Wake On LAN (WOL) supported
I/O Control	Via ITE IT8516E Embedded Controller via LPC Bus interface
Expansion Capabilities	• 1x PCIe x16 (Gen 2.0), 1x mPCIe (w. USB2.0) (KTH81/mITX) • 1x PCIe x16 (Gen 2.0 & 3.0), 1x mPCIe (w. USB2.0) (KTQ87/mITX) • 1x PCIe x16 (Gen 2.0), 1x PCIe x2 (x16 slot), 1x PCIe x1 (KTH81/Flex) • 1x PCIe x16 (Gen 2.0 & 3.0), 1x PCIe x4 (x16 slot), 1x PCIe x1 (KTQ87/Flex) • PCI (Flex only) • SMBus, compatible with ACCES BUS and I2C BUS, (via Feature connector) • SPI bus routed to SPI connector (BIOS Recovery module interface) • DDC/AUX Bus routed to DP connector (Auto detect to DDC when using passive DP to HDMI or DVI adapters) • 18 x GPIOs (General Purpose I/Os), (via Feature connector) • DAC, ADC, PWM and TIMER (Multiplexed), (via Feature connector) • WAKE UP / Interrupt Inputs (Multiplexed), (via Feature connector) • 3 Wire Bus for GPIO Expansion (up to 152 GPIOs), (via Feature connector) • 8 bit Timer output, (via Feature connector)
Hardware Monitor Subsystem	• Smart Fan control system, support Thermal® and Speed® cruise for two on-board Fan connectors: CPU Fan (on-board) and System Fan (on-board) • Thermal inputs: CPU Die temperature (precision +/- 3°C), System temperature (precision +/- 3°C) • Intrusion (Case Open) detect input, (via Feature connector) • Sleep S5# Indication, (via Feature connector) • System Powergood Signal, (via Feature connector)
Power Supply Unit	ATX/BTX (w. ATX+12V) PSU, 24-pin and 4-pin
Battery	Exchangeable 3.0V Lithium battery for on-board Real Time Clock and CMOS RAM. Manufacturer Panasonic / Part-number CR-2032L/BN, CR2032N/BN or CR-2032L/BE. Approximate 6.2 years retention. Current draw is less than 4.2µA when PSU is disconnected and 0 µA in S0 – S5. **CAUTION: Danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.**

Environmental Conditions	**Operating:** 0°C – 60°C operating temperature (forced cooling). It is the customer's responsibility to provide sufficient airflow around each of the components to keep them within allowed temperature range. 10% - 90% relative humidity (non-condensing) **Storage:** -20°C – 70°C; lower limit of storage temperature is defined by specification restriction of on-board CR2032 battery. Board with battery has been verified for storage temperature down to -40°C by Kontron. 5% - 95% relative humidity (non-condensing) **Electro Static Discharge (ESD) / Radiated Emissions (EMI):** All Peripheral interfaces intended for connection to external equipment are ESD/ EMI protected. EN 61000-4-2:2000 ESD Immunity EN55022:1998 class B Generic Emission Standard. **Safety:** IEC 60950-1: 2005, 2nd Edition UL 60950-1 CSA C22.2 No. 60950-1 Product Category: Information Technology Equipment Including Electrical Business Equipment Product Category CCN: NWGQ2, NWGQ8 File number: E194252 **Shock:** IAW IEC 60068-2-27, Test Ea, shock, 18 shocks 3 per axis, 6 directions. Shock pulse 50g, 11ms halfsine. **Bump:** IAW IEC 60068-2-29, Test Eb, Bump, 3000 bumps, 500 per axis, 6 directions. Half Sine Waveform Acceleration 2g; Pulse Duration 11ms. **Vibration:** IAW IEC 60068-2-64, Test Fh, Random Vibration. 90 min per axis, 3 axes, at 1.9 grms, with PSD: 10-20 Hz: 0.05 g^2/Hz and 20-500 Hz: -3dB/octave. **Theoretical MTBF:** 599.559 / 398.053 hours @ 40°C / 50°C for the mITX boards. 464.021 / 329.037 hours @ 40°C / 50°C for the Flex boards. **Restriction of Hazardous Substances (RoHS):** All boards in the KTQ87 / KTH81 family are RoHS compliant. **Capacitor utilization:** No Tantalum capacitors on board Only Japanese brand Solid capacitors rated for 100 °C used on board

3.2 System Overview

The block diagram below shows the architecture and main components of the KTQ87 / KTH81. The key component on the board is the Intel® Q87/H81 (Lynx Point) Desktop Platform controller Hub



3.3 Processor Support Table

KTQ87 is designed to support the following LGA1150 Desktop processors (up to 65W power consumption):

4rd generation Intel® Core™ i7 processor
4rd generation Intel® Core™ i5 processor
Haswell™ Dual Core Pentium
Haswell™ Duel Core Celeron

In the following list you will find all CPU's supported by the PCH in according to Intel but also other CPU's if successfully tested. Embedded CPU's are indicated by green text, successfully tested CPU's are indicated by **highlighted** text, successfully tested embedded CPU's are indicated by **green and highlighted** text and failed CPU's are indicated by red text. Some processors in the list are distributed from Kontron, those CPU's are marked by an * (asterisk). However please notice that this marking is only guide line and maybe not fully updated.

Processor Brand	Clock Speed [GHz]	Turbo Speed [GHz]	Cores	Threads	Bus Speed [MHz]	Cache [MB]	CPU Number	QDF/sSpec number	Stepping	Thermal Design Power [°C/W]
Core™ i7 4th gen.	3.2	4.0	4	8	1333/1600	8	4790S	SR1QM	C0	71/65
	3.1	**3.9**	**4**	**8**	**1333/1600**	**8**	**4770S**	**SR14H**	**C0**	**71/65**
	2.5	3.7	4	8	1333/1600	8	4770T	SR14N	C0	71/45
	2.3	3.3	4	8	1333/1600	8	4770TE	SR183	C0	71/45
	2.0	3.0	4	8	1333/1600	8	4765T	SR14Q	C0	66/35
Core™ i5 4th gen.	3.1	3.8	4	4	1333/1600	6	4670S	SR14K	C0	71/65
	3.0	3.7	4	4	1333/1600	4	4590S	SR1QN	C0	71/65
	2.9	**3.6**	**4**	**4**	**1333/1600**	**4**	**4570S**	**SR14J**	**C0**	**71/65**
	2.8	3.3	4	4	1333/1600	6	4440S	SR14L	C0	/65
	2.7	**3.2**	**4**	**4**	**1333/1600**	**6**	**4430S**	**SR14M**	**C0**	**71/65**
	2.3	3.3	4	4	1333/1600	6	4670T	SR14P	C0	71/45
	2.9	3.6	2	4	1333/1600	4	4570T	SR1CA	C0	66/35
	2.7	3.3	2	4	1333/1600	4	4570TE	SR17Z	C0	66/35
Core™ i3 4th gen.	3.6	-	2	4	1333/1600	4	4340	SR1NL	C0	72/54
	3.5	**-**	**2**	**4**	**1333/1600**	**4**	**4330**	**SR1NM**	**C0**	**72/54**
	3.4	-	2	4	1333/1600	3	4130	SR1NP	C0	72/54
	3.1	-	2	4	1333/1600	4	4350T	SR1PA	C0	66/35
	3.0	-	2	4	1333/1600	4	4330T	SR1NK	C0	66/35
	2.9	-	2	4	1333/1600	3	4130T	SR1NN	C0	66/35
	2.4	-	2	4	1333/1600	4	4330TE	SR180	C0	72/35
Haswell™ Dual Core Pentium	3.2	-	2	2	1333/1600	3	G3420	SR1NB	C0	72/54
	2.3	-	2	2	1333/1600	3	G3320TE	SR181	C0	72/35
Haswell™ Dual Core Celeron	2.7	-	2	2	1333	2	G1820	SR1CN	C0	/53
	2.2	-	2	2	1333	2	G1820TE	SR1T6	C0	/35

Note that ECC not supported on KTQ87 / KTH81.

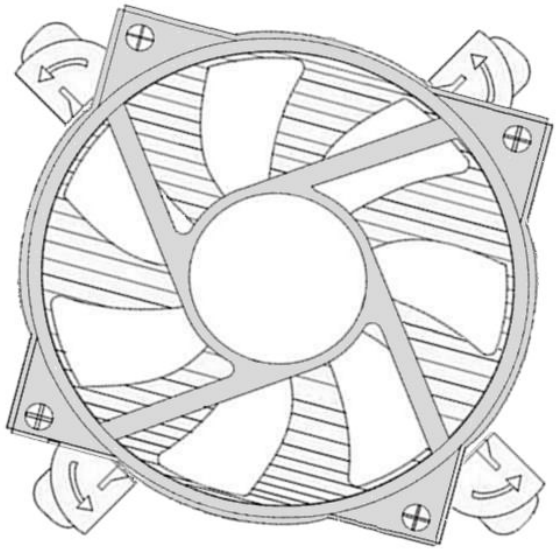
Not all CPU even of same type support all functions ex. i7-4770S & i5-4570S supports VPRO other CPU types may not. Intel® Turbo Boost Technology 2.0 is supported by i5 and i7, as indicated in above list of processors, and is enabling overclocking of all cores, when operated within the limits of thermal design power, temperature and current.

Note: KTH81 do not support VPRO.

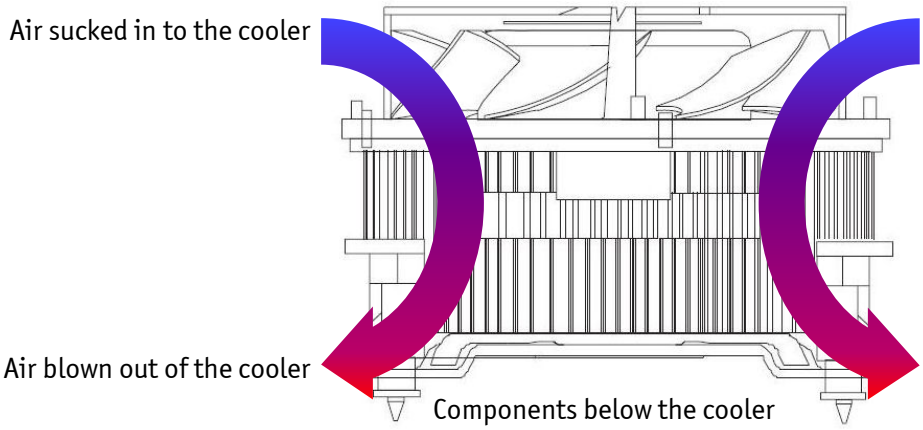
Sufficient cooling must be applied to the CPU in order to remove the effect as listed in above table (Thermal Guideline). The sufficient cooling is also depending on the maximum (worst-case) ambient operating temperature and the actual load of processor.

Warning: Make sure sufficient airflow is always present around the components located below the cooler. Different coolers are available on the market and some is not generating any airflow or is blocking the airflow around these components, causing reduced lifetime.

It is recommended to use a cooler like the Kontron PN 1046-6305 "KTQ77 Cooler".



The design of this cooler makes sure airflow is always present around the components below the cooler. Even if Fan is set to be off, it is still running a minimum RPM (Rotation Per Minute).



Note: The temperature of the air blown out of the cooler must be less than 60°C maximum, in order not to overheat components near the CPU. However most CPU's requires maximum 57,4°C, so in general, not to violate the CPU specification the temperature of the air should be maximum ~55°C. Some of the 65W CPU's running full load and cooled by above cooler, might start throttling at 50°C ambient air temperature.

3.4 System Memory support

The KTH81/mITX, KTQ87/mITX and KTH81/Flex have two DDR3 UDIMM sockets while the KTQ87/Flex has four DDR3 UDIMM sockets. The sockets support the following memory features:

- DDR3 1.5V/1.35V UDIMM 240-pin
- Dual-channel with 1 UDIMM per channel (2 UDIMM for KTQ87/Flex)
- Single/dual rank unbuffered 1333/1600MT/s (PC3-10600/PC3-12800)
- The supported 4rd Generation Core i5/i7 support 1333/1600 MT/s
- From 1GB and up to 2x 8GB (4x 8GB for KTQ87/Flex).
    - Note: Less than 4GB displayed in System Properties using 32bit OS
    - (Shared Video Memory/PCI resources is subtracted)
- SPD timings supported

The installed DDR3 DIMM should support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read and configure the memory controller for optimal performance. If non-SPD memory is used, the BIOS will attempt to configure the memory settings, but performance and reliability may be impacted.

Memory Operating Frequencies
Regardless of the DIMM type used, the memory frequency will either be equal to or less than the processor system bus frequency. For example, if DDR3 1600 memory is used with a 1333 MHz system bus frequency processor, the memory clock will operate at 167 MHz. The table below lists the resulting operating memory frequencies based on the combination of DIMMs and processor.

DIMM Type	Module name	Memory Data transfers [MT/s]	Processor system bus frequency [MHz]	Resulting memory clock frequency [MHz]	Peak transfer rate [MB/s]
DDR3 1333	PC3-10600	1333	1333 / 1600	167	10666
DDR3 1600	PC3-12800	1600	1333	167	10666
DDR3 1600	PC3-12800	1600	1600	200	12800

Notes: Kontron offers the following memory modules:

NEW SKU 04/2016*	SKU Name**	OLD SKU before 04/2016
1060-2492	DDR3-1333 DIMM 2GB	1054-3702
1060-2494	DDR3-1333 DIMM 4GB	1054-3703
1060-2496	DDR3-1333 DIMM 8GB	1054-3704
1060-2498	DDR3-1600 DIMM 2GB	1054-3707
1060-2500	DDR3-1600 DIMM 4GB	1054-3708
1060-2488	DDR3-1600 DIMM 8GB	1052-5601

*SKU changes were caused by administrative issues only, no hardware changes.
**Named are always the min. requirements, the shipped memory can fulfill a higher performance level

Memory modules have in general a much lower longevity than embedded motherboards, and therefor EOL of modules can be expected several times during lifetime of the motherboard. Kontron guarantees that the above P/N will be maintained so that EOL module will be replaced by other similar type of qualified module.

As a minimum it is recommend using Kontron memory modules for prototype system(s) in order to prove stability of the system and as for reference.

For volume production you might request to test and qualify other types of RAM. In order to qualify RAM it is recommend configuring 3 systems running RAM Stress Test program in heat chamber at 60^0C for a minimum of 24 hours.

3.5 KTQ87/KTH81 Graphics Subsystem

The KTQ87 / KTH81 equipped with Intel ® i5 or i7 processor supports Intel ® HD Graphics 4600.

KTQ87/KTH81 supports three/two DisplayPort directly from processor.

The DP interface supports the DisplayPort 1.2 specification. The PCH supports High-bandwidth Digital Content Protection for high definition content playback over digital interfaces. The PCH also integrates audio codecs for audio support over DP interfaces.

Up to three displays (any three display outputs: DP0, DP1 & DP2 can be activated at the same time and be used to implement independent or cloned display configuration. PCIe cards can be used to replace on-board graphics or in combination with on-board graphics.

Intel® HD Graphics 4600

Features of the Intel HD Graphics 4600 build into the i3, i5 and i7 processors, includes:

- High quality graphics engine supporting
  - 3 Symmetric Pipe Support
  - DirectX11.1 and OpenGL 4.x compliant and lower
  - Open CL 1.2 and lower
  - Core frequency of 350 - 1250 (Turbo) MHz
  - Memory Bandwidth up to 25.6 GB/s
  - Dynamic Video Memory Technology 5.0
  - DP 1.2 MST (Multi-Stream Transport)
  - PAVP
  - HDCP
  - Audio (Protected Content)
  - Full AVC/VC1/MPEG2 HW Decode and full MVC HW Decode

- DP0, DP1 & DP2
  - 16/32bit colours in WQXGA 3840x2160 @ 60 Hz.
  - Max HDMI resolution 4096x2304 @ 24 Hz
  - DisplayPort standard 1.2

- LVDS supports single and dual channel, 18/24bit VESA/JEIDA panels up to a resolution of 1600x1200 or 1920x1080 and with limited frame rate up to 1920x1200.

Display Configurations:

MB	LVDS	DP0 HDMI, DVI or DP	DP1 HDMI, DVI or DP	DP2 HDMI, DVI or DP
KTH81/mITX	No	Yes	Yes	No
KTQ87/mITX	No	Yes	Yes	Yes
KTH81/Flex	No	Yes	Yes	No
KTH81/Flex	Yes	Yes	No	No
KTQ87/Flex	No	Yes	Yes	Yes
KTQ87/Flex	Yes	Yes	No	Yes

Note the maximum resolutions:

LVDS	1920 x 1200 @ 60 Hz
HDMI	2560 x 1600 @ 60 Hz
DVI	1920 x 1200 @ 60 Hz
DP	3840 x 2160 @ 60 Hz

The HDMI and DVI limitations apply when using passive DP converter. When using Active DP converter the limitations depends on the converter, but maximum is 3840 x 2160 @ 60 Hz.

Graphics Adapters

Use of DP Adapter Converters can provide HDMI support or second VGA or DVI panel support.

The HDMI interface supports the HDMI 1.4a specification including audio codec. However limitations to the resolution apply: 1920x1080 (HDMI and DVI)

1051-7619 Cable DP Extender cable 200mm (when using two DP converters)

DP to VGA PN 1045-5779 DP to HDMI PN 1045-5781 DP to DVI- PN 1045-5780

Notice that only the DP to VGA adapter is an “active” converter, the HDMI and DVI converters are passive and cannot be used in a triple panel configuration.

3.6 Power Consumption

In order to ensure safe operation of the board, the ATX12V power supply must monitor the supply voltage and shut down if the supplies are out of range – refer to the hardware manual for the actual power supply specification. Please note, In order to keep the power consumption to a minimal level, boards do not implement a guaranteed minimum load. In some cases, this can lead to compatibility problems with ATX power supplies, which require a minimum load to stay in regulation. The KTQ87/mITX / KTH81/mITX board must powered through the ATX4P (4-pole) and the ATX24P (24-pole) connector using standard ATX power supply.

ATX12V supply: Both ATX4P connector and ATX24P connector must be used in according to the ATX12V PSU standard.

Warning: Hot Plugging power supply is not supported. Hot plugging might damage the board.

The requirements to the supply voltages are as follows:

Supply	Min	Max	Note
VCC3.3	3.135V	3.465V	Should be ±5% for compliance with the ATX specification
Vcc	4.75V	5.25V	Should be ±5% for compliance with the ATX specification. Should be +5/ -0% to meet the USB standard.
+12V	11.4V	12.6V	Should be ±5% for compliance with the ATX specification
–12V	–13.2V	–10.8V	Should be ±10% for compliance with the ATX specification
-5V	-5,50V	-4.5V	Not required for the KTQ87 boards
5VSB	4.75V	5.25V	Should be ±5% for compliance with the ATX specification

On the following pages you will find “total system power examples” for mITX and Flex boards in different configurations:

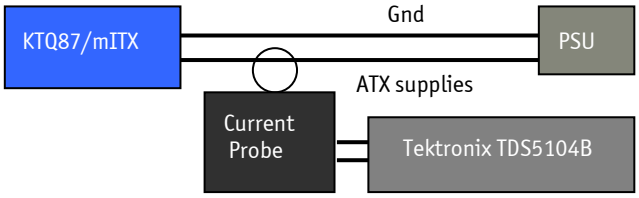
mITX, Total System power example:
- mITX, Low Power Configuration
- mITX, High Power Configuration

Flex, Total System power example:
- Flex, Low Power Configuration
- Flex, Medium Power Configuration
- Flex, High Power Configuration

mITX, Total System power example

The principal test system and test equipment used

1. Tektronix TDS5104B
2. Tektronix TCPA300
3. Tektronix TCP312
4. Fluke 289
5. Fluke 179
6. ATX rail switch



Note: Power consumption of PSU (power loss), Monitor and HDD are not included.

Low Power Configuration Setup KTQ87/mITX:
Standard system configuration equipped with Internal graphics, 2x SATA disks, mSATA 32GB, Intel 2.0Ghz CPU, 2x DIMM (8GB Modules), DVI Monitor, Keyboard & Mouse,1x 8GB USB Stick, 12V active cooler, 400W ATX PSU.

High Power Configuration Setup KTQ87/mITX:
Standard system configuration equipped with PCIex16 graphics card, mSATA 32GB, 4x SATA disks, Intel 2.5Ghz CPU, 2x DIMM (8GB Modules), DVI Monitor, Keyboard & Mouse, 4x 1-8GB USB Sticks, 12V active cooler, 400W ATX PSU.

Note: KTH81/mITX power results are similar to KTQ87/mITX.

mITX, Low Power Configuration results

DOS Idle, Mean, No external load		
Supply	Current draw [mA]	Power consumption [W]
+12V	96	1.158
+12V P4	1359	16.390
+5V	638	3.228
+3V3	491	1.664
-12V	21	0.236
5VSB	17	0.087
Total		**22.8**

Windows 7, mean 3DMARK2006 (first scene) + Burnin Test		
Supply	Current draw [mA]	Power consumption [W]
+12V	102	1.230
+12V P4	2420	29.185
+5V	1167	5.905
+3V3	494	1.675
-12V	22	0.247
5VSB	20	0.102
Total		**38.3**

S3 Mode, Mean, No external load		
Supply	Current draw [mA]	Power consumption [W]
5VSB	418	2.140
Total		**2.1**

S4 Mode, Mean, No external load		
Supply	Current draw [mA]	Power consumption [W]
5VSB	267	1.367
Total		**1.4**

S5 Mode, Mean, No external load		
Supply	Current draw [mA]	Power consumption [W]
5VSB	267	1.367
Total		**1.4**

mITX, High Power Configuration results

DOS Idle, Mean, No external load		
Supply	Current draw [mA]	Power consumption [W]
+12V	695	8.381
+12V P4	1820	21.949
+5V	902	4.564
+3V3	578	1.959
-12V	22	0.247
5VSB	20	0.102
Total		**37.2**

Windows 7, mean 3DMARK2006 (first scene) +Burnin test		
Supply	Current draw [mA]	Power consumption [W]
+12V	3320	40.039
+12V P4	3310	39.919
+5V	1145	5.794
+3V3	1121	3.800
-12V	18	0.202
5VSB	15	0.077
Total		**89.8**

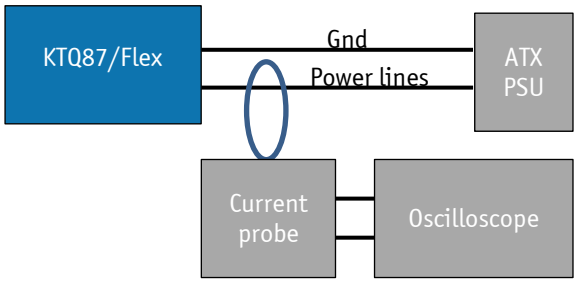
S3 Mode, Mean, No external load		
Supply	Current draw [mA]	Power consumption [W]
5VSB	429	2.196
Total		**2.2**

S4 Mode, Mean, No external load		
Supply	Current draw [mA]	Power consumption [W]
5VSB	273	1.398
Total		**1.4**

S5 Mode, Mean, No external load		
Supply	Current draw [mA]	Power consumption [W]
5VSB	269	1.377
Total		**1.4**

Flex, Total System power example

The principal test system and test equipment used



1. 12V active cooler (Delta AUC0912D)
2. USB Keyboard/Mouse (Lemel)
3. Graphic Card (HD 7750)
4. PCI Card (Intel 82557 10/100 ethernet pci adapter)
5. PCI-e Cards (TUSB7320 DEMO EVM REV C(PCIEx1 Card)
   Intel® 82575EB Gigabit Network Conection (PCIEx4 Card))
6. 3.5" HDD: WD WD500AAKX-001CA0, Seagate ST500DM002 & ST9160310AS, WD WD5000AAKX-00ERMA0
7. ATX 400W Power (GPB400S)
8. Oscilloscope (Tektronix DPO 4054)
9. Current Probe (Tektronix TCP0030 Current Probe)
10. USB Flash: Transcend JetFlash 4GB, ADATA C906 8GB, TDK 8GB, Kingston DTI/1G
11. Monitors: ASUS VS209N,ViewSonic VA1912MA-LED
12. Memory: SAMSUNG M391B1G73BH0-CK0 8GB PC3-12800E-11-11-E3
13. Intel Haswell CPU: QFZQ 2.20GHz (35W), QEEG 2.30GHz (45W), QE74 2.90GHz (65W)

Note: The power consumption of Display and HDD are not included.

Low Power Configuration Setup:

KTQ87/Flex equipped with Internal graphics, 2x SATA disks, PCI card, CPU (i5) 35W, 2x DIMM PC3-10600 (2x 2GB), 1x DP Monitor, Keyboard & Mouse. 1x 1-8GB USB Stick.

Medium Power Configuration Setup:
KTQ87/Flex equipped with Internal graphics, 4x SATA disks, PCI card, PCIex4 card, CPU (i5) 45W, 4x DIMM PC3-12800 (4x 4GB), 2x DP Monitors, Keyboard & Mouse. 2x 1-8GB USB Stick.

High Power Configuration Setup:
KTQ87/Flex equipped with PCIex16 Gen3 Graphic card, 4x SATA disks, PCI Card, PCIex1 card, PCIex4 card, CPU (i7) 65W, 4x DIMM PC3-12800 (4x 8Gb), 2x DP Monitors, Keyboard & Mouse, 4x 1-8GB USB Sticks

Note: KTH81/Flex power results are similar to KTQ87/Flex.

Flex, Low Power Configuration results

DOS Idle, Mean, No external load		
Supply	Current draw [mA]	Power consumption [W]
+12V	91	1.092
+12V P4	970	11.640
+5V	997	4.985
+3V3	739	2.439
-12V	11	0.132
5VSB	5	0.025
Total		**20.3**

Windows 7, mean 3DMARK2006 (first scene) +Burnin test		
Supply	Current draw [mA]	Power consumption [W]
+12V	101	1.212
+12V P4	2048	24.576
+5V	2027	10.135
+3V3	843	2.782
-12V	0	0
5VSB	8	0.040
Total		**38.7**

S3 Mode, Mean, No external load		
Supply	Current draw [mA]	Power consumption [W]
5VSB	286	1.43
Total		**1.4**

S4 Mode, Mean, No external load		
Supply	Current draw [mA]	Power consumption [W]
5VSB	130	0.715
Total		**0.7**

S5 Mode, Mean, No external load		
Supply	Current draw [mA]	Power consumption [W]
5VSB	123	0.677
Total		**0.7**

Flex, Medium Power Configuration results

DOS Idle, Mean, No external load		
Supply	Current draw [mA]	Power consumption [W]
+12V	154	1.848
+12V P4	1363	16.356
+5V	1083	5.415
+3V3	856	2.825
-12V	11	0.132
5VSB	8	0.040
Total		**26.6**

Windows 7, mean 3DMARK2006 (first scene) +Burnin test		
Supply	Current draw [mA]	Power consumption [W]
+12V	0 TBD	0 TBD
+12V P4	4100 TBD	49.200 TBD
+5V	2932	14.660
+3V3	867	2.861
-12V	0	0
5VSB	17	0.085
Total		**66.8**

S3 Mode, Mean, No external load		
Supply	Current draw [mA]	Power consumption [W]
5VSB	296	1.480
Total		**1.5**

S4 Mode, Mean, No external load		
Supply	Current draw [mA]	Power consumption [W]
5VSB	139	0.695
Total		**0.7**

S5 Mode, Mean, No external load		
Supply	Current draw [mA]	Power consumption [W]
5VSB	134	0.670
Total		**0.7**

Flex, High Power Configuration results

DOS Idle, Mean, No external load		
Supply	Current draw [mA]	Power consumption [W]
+12V	1285	15.420
+12V P4	1781	21.372
+5V	1175	5.875
+3V3	1530	5.049
-12V	12	0.144
5VSB	4	0.020
Total		**47.9**

Windows 7, mean 3DMARK2006 (first scene) +Burnin test		
Supply	Current draw [mA]	Power consumption [W]
+12V	2790	33.480
+12V P4	2880	34.560
+5V	1896	9.480
+3V3	1665	5.495
-12V	12	0.144
5VSB	10	0.050
Total		**83.2**

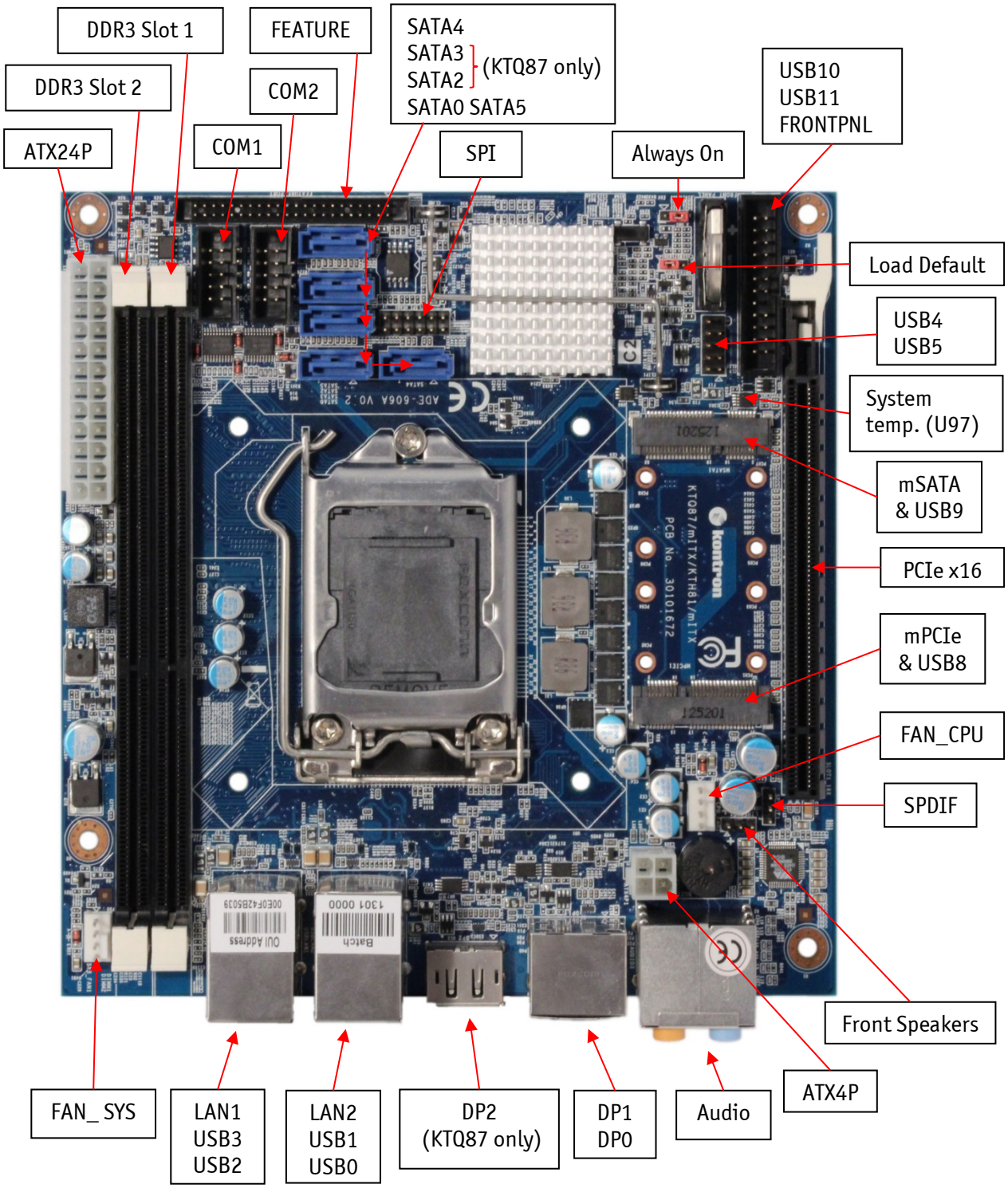
S3 Mode, Mean, No external load		
Supply	Current draw [mA]	Power consumption [W]
5VSB	296	1.480
Total		**1.5**

S4 Mode, Mean, No external load		
Supply	Current draw [mA]	Power consumption [W]
5VSB	168	0.840
Total		**0.8**

S5 Mode, Mean, No external load		
Supply	Current draw [mA]	Power consumption [W]
5VSB	134	0.670
Total		**0.7**

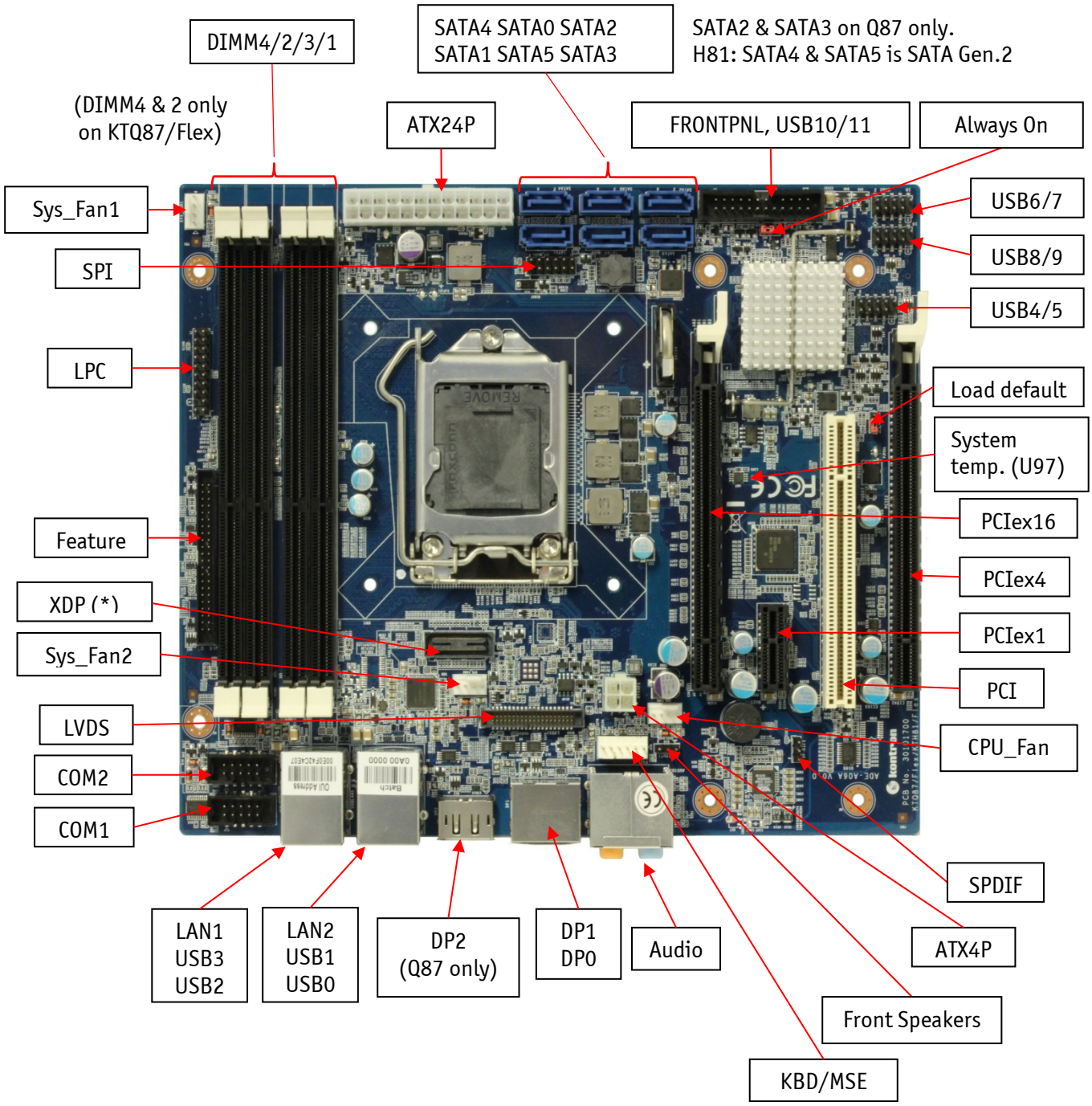
4 Connector Locations

4.1 KTQ87/mITX (KTH81/mITX) - frontside



KTH81 Notes:
USB port 2 & 3 only supports USB 2.0.
SATA4 & SATA5 connectors are black colored and limited to SATA 300.

4.2 KTQ87/Flex (KTH81/Flex) - frontside



(*) = Not Mounted.

5 Connector Definition

The following sections provide pin definitions and detailed description of all on-board connectors.

The connector definitions follow the following notation:

Column name	Description
Pin	Shows the pin-numbers in the connector. The graphical layout of the connector definition tables is made similar to the physical connectors.
Signal	The mnemonic name of the signal at the current pin. The notation "XX#" states that the signal "XX" is active low.
Type	AI: Analogue Input. AO: Analogue Output. I: Input, TTL compatible if nothing else stated. IO: Input / Output. TTL compatible if nothing else stated. IOT: Bi-directional tristate IO pin. IS: Schmitt-trigger input, TTL compatible. IOC: Input / open-collector Output, TTL compatible. IOD: Input / Output, CMOS level Schmitt-triggered. (Open drain output) NC: Pin not connected. O: Output, TTL compatible. OC: Output, open-collector or open-drain, TTL compatible. OT: Output with tri-state capability, TTL compatible. LVDS: Low Voltage Differential Signal. PWR: Power supply or ground reference pins.
	Ioh: Typical current in mA flowing out of an output pin through a grounded load, while the output voltage is > 2.4 V DC (if nothing else stated). Iol: Typical current in mA flowing into an output pin from a VCC connected load, while the output voltage is < 0.4 V DC (if nothing else stated).
Pull U/D	On-board pull-up or pull-down resistors on input pins or open-collector output pins.
Note	Special remarks concerning the signal.

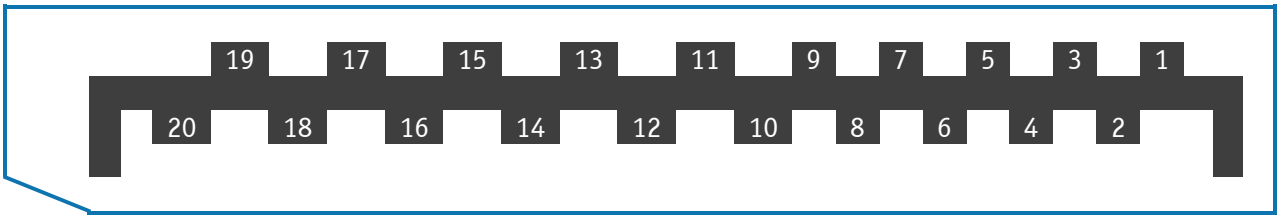
The abbreviation *TBD* is used for specifications which are not available yet or which are not sufficiently specified by the component vendors.

6 IO-Area Connectors

6.1 DP Connectors (DP0, DP1, DP2)

The DP (DisplayPort) connectors are based on standard DP type Foxconn 3VD51203-H7JJ-7H or similar.

Note that DP2 only available on KTQ87.



Pin	Signal	Description	Type	Note
1	Lane 0 (p)		LVDS	
2	GND		PWR	
3	Lane 0 (n)		LVDS	
4	Lane 1 (p)		LVDS	
5	GND		PWR	
6	Lane 1 (n)		LVDS	
7	Lane 2 (p)		LVDS	
8	GND		PWR	
9	Lane 2 (n)		LVDS	
10	Lane 3 (p)		LVDS	
11	GND		PWR	
12	Lane 3 (n)		LVDS	
13	Config1	Aux or DDC selection	I	Internally pull down (1Mohm). Aux channel on pin 15/17 selected as default (when NC) DDC channel on pin 15/17, If HDMI adapter used (3.3V)
14	Config2	(Not used)	O	Internally connected to GND
15	Aux Ch (p)	Aux Channel (+) or DDC Clk		AUX (+) channel used by DP DDC Clk used by HDMI
16	GND		PWR	
17	Aux Ch (n)	Aux Channel (-) or DDC Data		AUX (-) channel used by DP DDC Data used by HDMI
18	Hot Plug		I	Internally pull down (100Kohm).
19	Return		PWR	Same as GND
20	3.3V		PWR	Fused by 1.5A resetable PTC fuse.

6.2 Ethernet Connectors

The KTQ87/KTH81 supports two channels of 10/100/1000Mb Ethernet. First Ethernet connector (LAN1) is based on Intel® Clarkville i218LM/i218-V Gigabit PHY. The i218-LM (Q87) has AMT 9.0 support and the i218-V (H81) has no AMT support. Second Ethernet connector (LAN2) is based on Intel® Pearsonville i218AT PCI Express controller.

In order to achieve the specified performance of the Ethernet port, Category 5 twisted pair cables must be used with 10/100MB and Category 5E, 6 or 6E with 1Gb LAN networks.

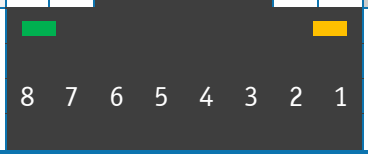
The signals for the Ethernet ports are as follows:

Signal	Description
MDI[0]+ / MDI[0]-	In MDI mode, this is the first pair in 1000Base-T, i.e. the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDI[1]+ / MDI[1]-	In MDI mode, this is the second pair in 1000Base-T, i.e. the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDI[2]+ / MDI[2]-	In MDI mode, this is the third pair in 1000Base-T, i.e. the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair.
MDI[3]+ / MDI[3]-	In MDI mode, this is the fourth pair in 1000Base-T, i.e. the BI_DD+/- pair. In MDI crossover mode, this pair acts as the BI_DC+/- pair.

Note: MDI = Media Dependent Interface.

Ethernet LAN1 is mounted together with USB Ports 2 and 3.
Ethernet LAN2 is mounted together with USB Ports 0 and 1.

The pinout of the RJ45 connectors is as follows:

Signal	PIN	Type	Ioh/Iol	Note
MDI0+				
MDI0-				
MDI1+				
MDI2+				
MDI2-				
MDI1-				
MDI3+				
MDI3-				
Flashing => communication		On => 1GB link		

6.3 USB Connectors (IO Area)

The KTQ87 board contains two EHCI (Enhanced Host Controller Interface) and one XHCI (Extensible Host Controller Interface). The two EHCI controllers, EHCI1 and EHCI2, supports up to fourteen USB 2.0 ports allowing data transfers up to 480Mb/s. The XHCI controller supports six USB 3.0 ports allowing data transfers up to 5Gb/s. The six USB 3.0 ports are shared with four of the USB 2.0 ports (USB0 – USB3) from the EHCI1.

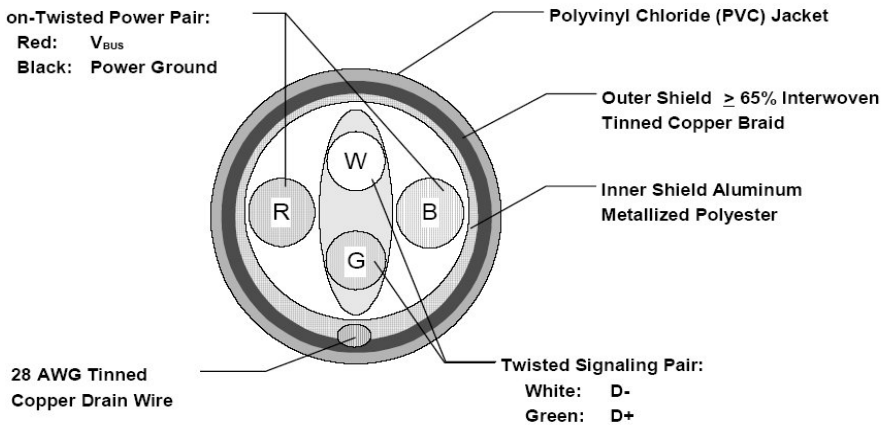
Note: Not all USB 2.0 and USB 3.0 ports are physically connected to the board.

The KTQ87/mITX has total of 10 USB ports where four ports support USB 3.0 or USB 2.0 via Rear IO connectors. The KTH81/mITX has total of 10 USB ports where two ports support USB 3.0 or USB 2.0 via Rear IO connectors (USB port 2 & 3 in Rear IO only supports USB 2.0).
The KTQ87/Flex has total of 12 USB ports where four ports support USB 3.0 or USB 2.0 via Rear IO connectors. The KTH81/mITX has total of 10 USB ports where two ports support USB 3.0 or USB 2.0 via Rear IO connectors (USB port 2 & 3 in Rear IO only supports USB 2.0).

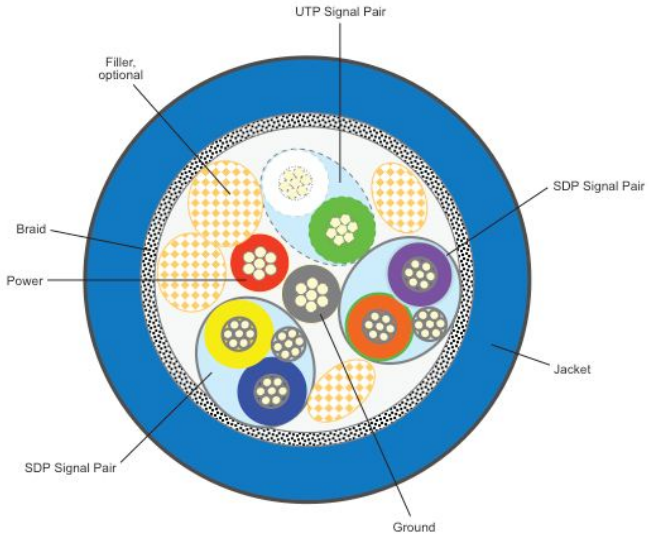
Legacy Keyboard/Mouse and wakeup from sleep states are supported. Over-current detection on all USB ports is supported. The following USB connectors are available in the IO Area.

USB Port 0 and 1 (via EHCI1/XHCI) are supplied on the combined USB0, USB1 and LAN2 connector.
USB Port 2 and 3 (via EHCI1/XHCI) are supplied on the combined USB2, USB3 and LAN1 connector.

For USB2.0 cabling it is required to use only HiSpeed USB cable, specified in USB2.0 standard:



For USB3.0 cabling it is required to use only HiSpeed USB cable, specified in USB3.0 standard:



USB Connector 0/1 (USB0/1)

USB Ports 0 and 1 are mounted together with LAN2 port and supports USB3.0/USB2.0.

Note	Type	Signal	PIN	Signal	Type	Note
	IO		USB1- USB1+		IO	
1	PWR	5V/SB5V	1 2 3 4	GND	PWR	
	IO	RX1-	5 6 7 8 9	TX1+	IO	
	IO		RX1+ TX1-		IO	
	PWR		GND			
	IO		USB0- USB0+		IO	
1	PWR	5V/SB5V	1 2 3 4	GND	PWR	
	IO	RX0-	5 6 7 8 9	TX0+	IO	
	IO		RX0+ TX0-		IO	
	PWR		GND			

Note 1: In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

Signal	Description
USBn+ USBn- RXn+ RXn- TXn+ TXn- (n= 0,1)	Differential pair works as serial differential receive/transmit data lines.
5V/SB5V	5V supply for external devices. SB5V is supplied during power-down to allow wakeup on USB device activity. Protected by resettable 2A fuse covering both USB ports.

USB Connector 2/3 (USB2/3)

USB Ports 2 and 3 are mounted together with LAN1 port and supports USB3.0/USB2.0.

Note	Type	Signal	PIN					Signal	Type	Note
	IO				USB3-		USB3+		IO	
1	PWR	5V/SB5V	1	2	3	4		GND	PWR	
	IO	RX3-	5	6	7	8	9	TX3+	IO	
	IO				RX3+			TX3-	IO	
	PWR				GND					
	IO				USB2-		USB2+		IO	
1	PWR	5V/SB5V	1	2	3	4		GND	PWR	
	IO	RX2-	5	6	7	8	9	TX2+	IO	
	IO				RX2+			TX2-	IO	
	PWR				GND					

Note 1: In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

Signal	Description
USBn+ USBn- RXn+ RXn- TXn+ TXn- (n= 2,3)	Differential pair works as serial differential receive/transmit data lines.
5V/SB5V	5V supply for external devices. SB5V is supplied during power-down to allow wakeup on USB device activity. Protected by resettable 2A fuse covering both USB ports.

6.4 Audio Jack Connector Stack (Audio)

The on-board Audio circuit implements up to 8 Channel High Definition Audio via stacked audiojack connectors and via SPDIF connector, see SPDIF description.

Interface is based on UAA (Universal Audio Architecture), featuring five 24-bit stereo DACs and three 20-bit stereo ADCs. Beside 8 channels audio signal the stached audiojack connectors include Line-in (left and right) and Microphone (left and right).

Note	Type	Signal			Signal	Type	Note
	OA	CEN-OUT	TIP RING SLEEVE	TIP RING SLEEVE	LINE1-IN-L	IA	
	OA	LFE-OUT			LINE1-IN-R	IA	
	PWR	GND			GND	PWR	
	OA	REAR-OUT-L	TIP RING SLEEVE	TIP RING SLEEVE	FRONT-OUT-L	OA	
	OA	REAR-OUT-R			FRONT-OUT-R	OA	
	PWR	GND			GND	PWR	
	OA	SIDE-OUT-L	TIP RING SLEEVE	TIP RING SLEEVE	MIC1-L	IA	
	OA	SIDE-OUT-R			MIC1-R	IA	
	PWR	GND			GND	PWR	

Signal	Description	Note
FRONT-OUT-L	Front Speakers (Speaker Out Left).	Shared w. 3-pin connector (LINEOUT)
FRONT-OUT-R	Front Speakers (Speaker Out Right).	Shared w. 3-pin connector (LINEOUT)
REAR-OUT-L	Rear Speakers (Surround Out Left).	N/A
REAR-OUT-R	Rear Speakers (Surround Out Right).	N/A
SIDE-OUT-L	Side speakers (Surround Out Left)	N/A
SIDE-OUT-R	Side speakers (Surround Out Right)	N/A
CEN-OUT	Center Speaker (Center Out channel).	N/A
LFE-OUT	Subwoofer Speaker (Low Freq. Effect Out).	N/A
MIC1	MIC Input 1	N/A
LINE1-IN	Line in 1 signals	N/A

Port	2-channel	4-channel	6-channel	8-channel
Light Blue	Line in	Line in	Line in	Line in
Lime	Line out	Front speaker out	Front speaker out	Front speaker out
Pink	Mic in	Mic in	Mic in	Mic in
Audio header	-	-	-	Side speaker out
Audio header	-	Rear speaker out	Rear speaker out	Rear speaker out
Audio header	-	-	Center/ Subwoofer	Center/ Subwoofer

7 Internal Connectors

The KTQ87/KTH81 boards are designed to be supplied from a standard ATX (or BTX) power supply. Use of BTX supply is not required for operation, but may be required to drive high-power PCIe cards.

Warning: Hot plugging any of the two power connectors is not allowed. Hot plugging might damage the board. In other words, turn off main supply etc. to makesure all the power lines (+12V, 5V, SB5V, 3.3V, -5V, -12V) are turned off when connecting to the motherboard.

Note 1: Use of both the ATX24P and the ATX4p connectors are required for operation of the KTQ87/KTH81.

7.1 Power Connector (ATX24P)

Note	Type	Signal	PIN		Signal	Type	Note
	PWR	3V3	12	24	GND	PWR	
	PWR	+12V	11	23	5V	PWR	
	PWR	+12V	10	22	5V	PWR	
	PWR	SB5V	9	21	5V	PWR	
	I	P_OK	8	20	-5V	PWR	1
	PWR	GND	7	19	GND	PWR	
	PWR	5V	6	18	GND	PWR	
	PWR	GND	5	17	GND	PWR	
	PWR	5V	4	16	PSON#	OC	
	PWR	GND	3	15	GND	PWR	
	PWR	3V3	2	14	-12V	PWR	
	PWR	3V3	1	13	3V3	PWR	

See chapter “Power Consumption” regarding input tolerances on 3.3V, 5V, SB5V, +12 and -12V (also refer to ATX specification version 2.2).

Signal	Description
P_OK	P_OK is power good signal driven by the ATX Power Supply and indicating that the +5VDC and +3.3VDC outputs are above the undervoltage thresholds. The recommended electrical and timing characteristics of the P_OK (PWR_OK) signal are provided in the *ATX12V Power SupplyDesign Guide*. It is strongly recommended to use an ATX or BTX supply, in order to provide supervision of the 5V and 3V3 supplies. These supplies are not supervised on-board.
PS_ON#	Active low open drain signal from the board to the power supply to turn on the power supply outputs. Signal must be pulled high by the power supply.

7.2 Power Connector (ATX4p)

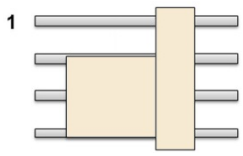
Note	Type	Signal	PIN		Signal	Type	Note
	PWR	GND	2	4	+12V	PWR	1
	PWR	GND	1	3	+12V	PWR	1

7.3 Fan Connectors (CPU_Fan, SYS_Fan1, SYS_Fan2)

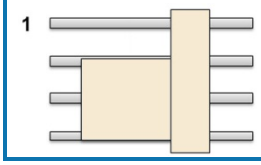
The SYS_FAN1 and SYS_Fan2 can be used to power, control and monitor fans for chassis ventilation etc. The CPU_Fan is used for the connection of the FAN included in active CPU coolers.

The 4pin header is recommended to be used for driving 4-wire type Fan in order to implement FAN speed control. 3-wire Fan support is also possible, but no fan speed control is integrated.

4-pin Mode:

Header	Pin	Signal	Description	Type
	1	PWM	PWM output	0-3.3
	2	TACHO	Tacho signal	I
	3	12V	Power +12V	PWR
	4	GND	Ground	PWR

3-pin Mode:

Header	Pin	Signal	Description	Type
	1		Not used	
	2	TACHO	Tacho signal	I
	3	12V	Power +12V	PWR
	4	GND	Ground	PWR

Signal	Description
PWM	PWM output signal for FAN speed control.
TACHO	Tacho input signal from the fan, for rotation speed supervision RPM (Rotation Per Minute). The signal shall be generated by an open collector transistor or similar. Onboard is a pull-up resistor 4K7 to +12V. The signal has to be pulsed and onboard circuit is prepared for two pulses per rotation.
12V	+12V supply for fan. A maximum of 2000mA can be supplied from this pin.
GND	Power Supply GND signal

7.4 PS/2 Keyboard and Mouse Connector (KBD/MSE) (PS2)

Attachment of a PS/2 keyboard/mouse can be done through the pinrow connector KBD/MSE (Flex boards only). Both interfaces utilize open-drain signalling with on-board pull-up.

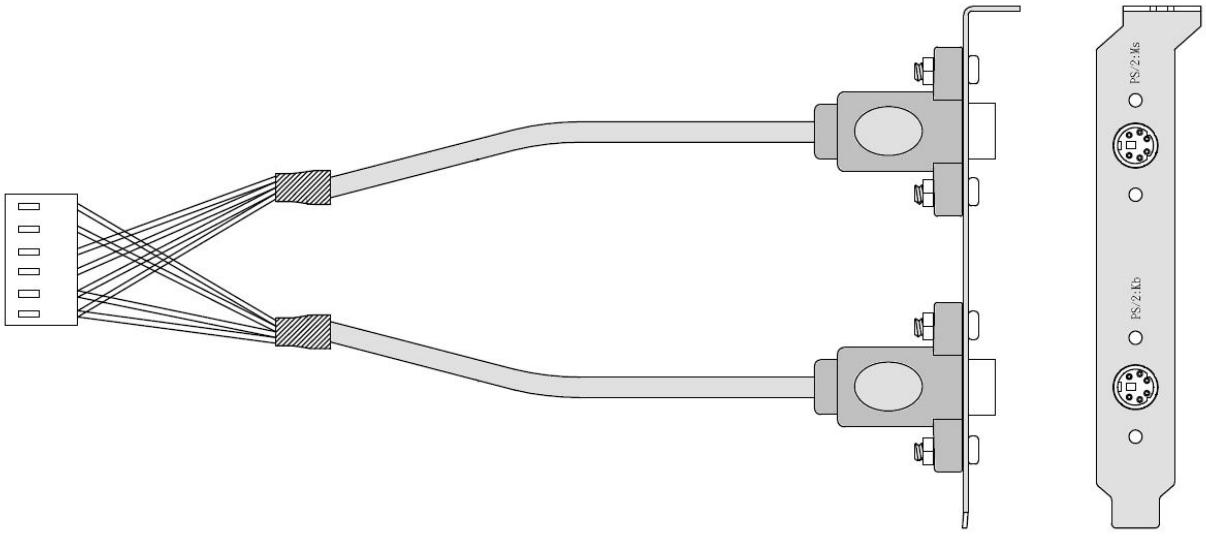
The PS/2 mouse and keyboard is supplied from SB5V when in standby mode in order to enable keyboard or mouse activity to bring the system out from power saving states. The supply is provided through a 1.1A resettable fuse.

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	KBDCLK	IOD	/14mA	2K7	
2	KBDDAT	IOD	/14mA	2K7	
3	MSCLK	IOD	/14mA	2K7	
4	MSDAT	IOD	/14mA	2K7	
5	5V/SB5V	PWR	-	-	
6	GND	PWR	-	-	

Signal Description – Keyboard & and mouse Connector (KBDMSE).

Signal	Description
MSCLK	Bi-directional clock signal used to strobe data/commands from/to the PS/2 mouse.
MSDAT	Bi-directional serial data line used to transfer data from or commands to the PS/2 mouse.
KDBCLK	Bi-directional clock signal used to strobe data/commands from/to the PC-AT keyboard.
KBDDAT	Bi-directional serial data line used to transfer data from or commands to the PC-AT keyboard.

Available cable kit:



PN 1053-2384 Bracket Cable 6-Pin to PS2-Kbd-Mse

7.5 LVDS Flat Panel Connector (LVDS)

The LVDS connector (Flex boards only) is based on 40 pole connector type Samtec SHF-120-01-F-D-SM-K-TR or similar.

Note	Type	Signal	PIN		Signal	Type	Note
Max. 0.5A	PWR	+12V	1	2	+12V	PWR	Max. 0.5A
Max. 0.5A	PWR	+12V	3	4	+12V	PWR	Max. 0.5A
Max. 0.5A	PWR	+12V	5	6	GND	PWR	Max. 0.5A
Max. 0.5A	PWR	+5V	7	8	GND	PWR	Max. 0.5A
Max. 0.5A	PWR	LCDVCC	9	10	LCDVCC	PWR	Max. 0.5A
2K2Ω, 3.3V	OT	DDC CLK	11	12	DDC DATA	OT	2K2Ω, 3.3V
3.3V level	OT	BKLTCTL	13	14	VDD ENABLE	OT	3.3V level
3.3V level	OT	BKLTEN#	15	16	GND	PWR	Max. 0.5A
	LVDS	LVDS A0-	17	18	LVDS A0+	LVDS	
	LVDS	LVDS A1-	19	20	LVDS A1+	LVDS	
	LVDS	LVDS A2-	21	22	LVDS A2+	LVDS	
	LVDS	LVDS ACLK-	23	24	LVDS ACLK+	LVDS	
	LVDS	LVDS A3-	25	26	LVDS A3+	LVDS	
Max. 0.5A	PWR	GND	27	28	GND	PWR	Max. 0.5A
	LVDS	LVDS B0-	29	30	LVDS B0+	LVDS	
	LVDS	LVDS B1-	31	32	LVDS B1+	LVDS	
	LVDS	LVDS B2-	33	34	LVDS B2+	LVDS	
	LVDS	LVDS BCLK-	35	36	LVDS BCLK+	LVDS	
	LVDS	LVDS B3-	37	38	LVDS B3+	LVDS	
Max. 0.5A	PWR	GND	39	40	GND	PWR	Max. 0.5A

Note: The LVDS connector supports single and dual channel, 18/24bit SPWG panels up to a resolution of 1600x1200 or 1920x1080 and with limited frame rate up to 1920x1200.

Signal Description – LVDS Flat Panel Connector:

Signal	Description
LVDS A0..A3	LVDS A Channel data
LVDS ACLK	LVDS A Channel clock
LVDS B0..B3	LVDS B Channel data
LVDS BCLK	LVDS B Channel clock
BKLTCTL	Backlight control (1), PWM signal to implement voltage in the range 0-3.3V
BKLTEN#	Backlight Enable signal (active low) (2)
VDD ENABLE	Output Display Enable.
LCDVCC	VCC supply to the display. 5V or 3.3V (1A Max.) selected in BIOS setup menu. Power sequencing depends on LVDS panel selection. (Shared with eDP connector)
DDC CLK	DDC Channel Clock

Notes: Windows API will be available to operate the BKLTCTL signal. Some Inverters have a limited voltage range 0- 2.5V for this signal: If voltage is > 2.5V the Inverter might latch up. Some Inverters generates noise on the BKLTCTL signal, causing the LVDS transmission to fail (corrupted picture on the display). By adding a 1Kohm resistor in series with this signal, mounted at the Inverter end of the cable kit, the noise is limited and the picture is stable.
If the Backlight Enable is required to be active high then, check the following BIOS Chipset setting: Backlight Signal Inversion = Enabled.

7.6 SATA (Serial ATA) Disk Interface

KTQ87 / KTH81 has integrated SATA Host controller (PCH in the Q87 / H81 chipset) which supports independent DMA operation on 6 / 4 ports. One device can be installed on each port, via point-to-point interface (SATA cable), for a maximum of 6 / 4 SATA devices. On the mITX the SATA ports are available as 5 / 3 SATA connectors + 1 mSATA connector and on the Flex the SATA ports are available as 6 / 4 SATA connectors.

All the SATA ports on the Q87 support SATA Gen3 (6.0/3.0/1.5Gb/s) are supported, while two SATA ports on the H81 supports Gen3 and the remaining two ports support Gen2 (3.0/1.5Gb/s).

Note: Before installing OS on a SATA drive make sure the drive is not a former member of a RAID system. If so some hidden data on the disk has to be erased. To do this, connect two SATA drives and select RAID in BIOS. Save settings and select <Ctrl> <I> while booting to enter the RAID setup menu. Now the hidden RAID data will be erased from the selected SATA drive.

Note: KTH81 do not support RAID.

The SATA controller supports:

- 2 to 6-drive RAID 0 (data striping)
- 2-drive RAID 1 (data mirroring)
- 3 to 6-drive RAID 5 (block-level striping with parity).
- 4-drive RAID 10 (data striping and mirroring)
- 2 to 6-drive matrix RAID, different parts of a single drive can be assigned to different RAID devices.
- AHCI (Advanced Host Controller Interface)
- NCQ (Native Command Queuing). NCQ is for faster data access.
- Swap bay support (not supported on mSATA)
- Intel® Rapid Recover Technology
- 2 – 256TB volume (Data volumes only)
- Capacity expansion
- TRIM in Windows 7 (in AHCI and RAID mode for drives not part of a RAID volume). (TRIM is for SSD data garbage handling).

Sata connector pinning: SATA0, SATA1, SATA2, SATA3, SATA4 and SATA5. (SATA1 used by mSATA on mITX)

PIN	Signal	Type	Ioh/Iol	Note
1	GND	PWR	-	
2	SATA* TX+			
3	SATA* TX-			
4	GND	PWR	-	
5	SATA* RX-			
6	SATA* RX+			
7	GND	PWR	-	

Signal	Description
SATA* RX+ / RX-	Host transmitter differential signal pair
SATA* TX+ / TX-	Host receiver differential signal pair

"*" specifies 0, 1, 2, 3, 4, 5 depending on SATA port.

Available cable kit:

PN 821035 Cable SATA 500mm

7.7 USB Connectors (USB)

The KTQ87 board contains two EHCI (Enhanced Host Controller Interface) host controllers (EHCI1 and EHCI2) and a XHCI (Extensible Host Controller Interface). The EHCI controllers support up to fourteen USB 2.0 ports allowing data transfers up to 480Mb/s and the XHCI controller supports up to six USB 3.0 ports allowing data transfers up to 5Gb/s. Four of the USB 3.0 ports are shared with four of the USB 2.0 ports (USB0 – USB3).

Note: Not all USB 2.0 and USB 3.0 ports are physically connected to the board.

Legacy Keyboard/Mouse and wakeup from sleep states are supported. Over-current detection on all fourteen USB ports is supported.

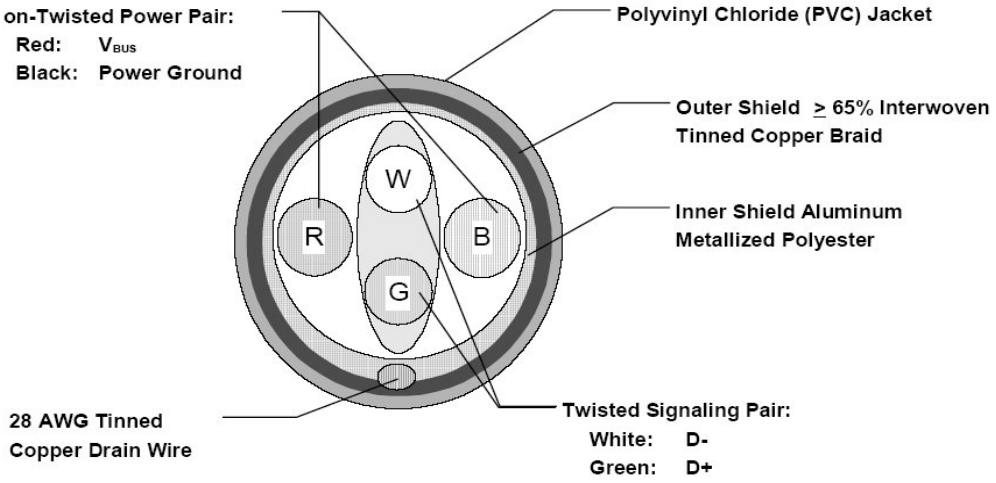
Notes:
On KTQ87, the four USB 3.0 ports (USB0 – USB3) are shared with four of the EHCI1 USB 2.0 ports.
On KTH81, the two USB 3.0 ports (USB0 – USB1) are shared with two of the EHCI1 USB 2.0 ports.
KTH81 only supports two USB 3.0 ports.

See chapter “USB Connectors (IO Area)” for more information on USB0 – USB3.

The following USB ports are available on Internal Pinrows:

USB 4 & 5 (via EHCI1) are supplied on USB4/5 internal pinrow connector (USB1).
USB 6 & 7 (via EHCI1) are supplied on USB6/7 internal pinrow connector (USB2). (KTQ87/Flex only).
USB 8 & 9 (via EHCI2):
Flex: are supplied on the USB8/9 internal pinrow connector (USB3).
mITX: USB8 is supplied on the mPCIe slot and USB9 is supplied on mSATA slot.
USB Port 10 and 11 (via EHCI2) are supplied on the USB10/11 internal pinrow FRONTPNL connector.

Note: It is required to use only HiSpeed USB cable, specified in USB2.0 standard:



USB 4 & 5 (USB4/5) (USB1)

USB Ports 4 and 5 are supplied on the internal USB4/5 pinrow connector USB1.

Note	Type	Signal	PIN		Signal	Type	Note
1	PWR	5V/SB5V	1	2	5V/SB5V	PWR	1
	IO	USB8-	3	4	USB9-	IO	
	IO	USB8+	5	6	USB9+	IO	
	PWR	GND	7	8	GND	PWR	
	NC	KEY	9	10	NC	NC	

USB 6 & 7 (USB6/7) (USB2)

USB Ports 6 and 7 are supplied on the internal USB6/7 pinrow connector USB1. (KTQ87/Flex only).

Note	Type	Signal	PIN		Signal	Type	Note
1	PWR	5V/SB5V	1	2	5V/SB5V	PWR	1
	IO	USB8-	3	4	USB9-	IO	
	IO	USB8+	5	6	USB9+	IO	
	PWR	GND	7	8	GND	PWR	
	NC	KEY	9	10	NC	NC	

USB 8 & 9 (USB8/9) (USB3)

USB Ports 6 and 7 are supplied on the internal USB6/7 pinrow connector USB1. (Flex only).

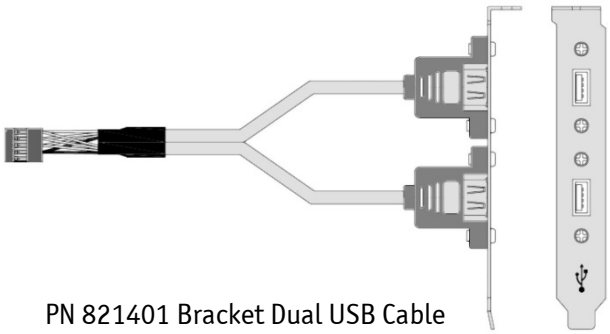
Note	Type	Signal	PIN		Signal	Type	Note
1	PWR	5V/SB5V	1	2	5V/SB5V	PWR	1
	IO	USB8-	3	4	USB9-	IO	
	IO	USB8+	5	6	USB9+	IO	
	PWR	GND	7	8	GND	PWR	
	NC	KEY	9	10	NC	NC	

Note1:

Signal	Description
USBx+ USBx-	Differential pair works as Data/Address/Command Bus.
5V/SB5V	5V supply for external devices. SB5V is supplied during powerdown to allow wakeup on USB device activity. Each 5V protected by resettable 1A fuse.

In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

Available cable kit:



PN 821401 Bracket Dual USB Cable

7.8 Serial COM1 – COM2 Ports (COM1, COM2)

Two RS232 serial ports are available on the KTQ87/KTH81.

The typical definition of the signals in the COM ports is as follows:

Signal	Description
TxD	Transmitted Data, sends data to the communications link. The signal is set to the marking state (-12V) on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RxD	Received Data, receives data from the communications link.
DTR	Data Terminal Ready, indicates to the modem etc. that the on-board UART is ready to establish a communication link.
DSR	Data Set Ready, indicates that the modem etc. is ready to establish a communications link.
RTS	Request To Send, indicates to the modem etc. that the on-board UART is ready to exchange data.
CTS	Clear To Send, indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect, indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator, indicates that the modem has received a ringing signal from the telephone line.

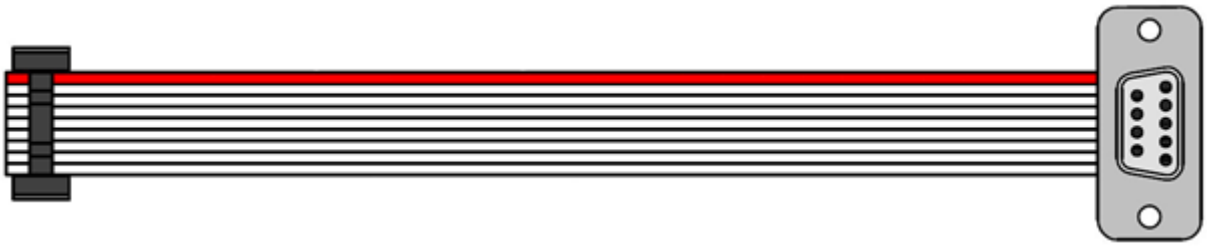
The pinout of Serial ports COM1 (J19), COM2 (J18)

Note	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Note
	-	I	DCD	1	2	DSR	I	-	
	-	I	RxD	3	4	RTS	O		
		O	TxD	5	6	CTS	I	-	
		O	DTR	7	8	RI	I	-	
	-	PWR	GND	9	10	5V	PWR	-	1

Note 1: The COM1, COM2 5V supply is fused with common 1.5A resettable fuse.

DB9 adapter cables (PN 821016 200mm long and 821017 100mm long) are available for implementing standard COM ports on chassis.

Available cable kit (DB9 adapter cables):



PN 821017 - 100 mm or PN 821016 - 200 mm

7.9 Audio Connectors

The on-board Audio circuit implements 7.1+2 Channel High Definition Audio with UAA (Universal Audio Architecture), featuring five 24-bit stereo DACs and three 20-bit stereo ADCs.

The following Audio connectors are available as Internal connectors.

Headphone and Mic2

Headphone and Mic2 are accessible via Front Panel Connector, see Front Panel Connector description.

Front Speakers (LINEOUT)

The Front Speakers (Left and Right) interface is available through 3-pin connector. These outputs are shared with the Speaker Audio Jack connector (green).
Up to 100 dB Signal-to-Noise Ratio (SNR).

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	Front Speaker-R		-	-	
2	GND	PWR	-	-	
3	Front Speaker -L	-	-	-	

SPDIF (SP-DIF)

The digital audio interface (electrical SPDIF-Out) is available through 3-pin connector and can be used to implement 8 (7.1) Channel High Definition Audio.

Circuit is based on high fidelity 8-channel HD audio codec which is compatible with Intel HD Audio specification and supports stereo 24-bit resolution and up to 192 kHz sample rate for DACs/ADCs.
Up to 90 dB Signal-to-Noise Ratio (SNR).

16/20/24-bit S/PDIF TX Outputs supporting 48K/96K/44.1K/88.2 KHz sample rate

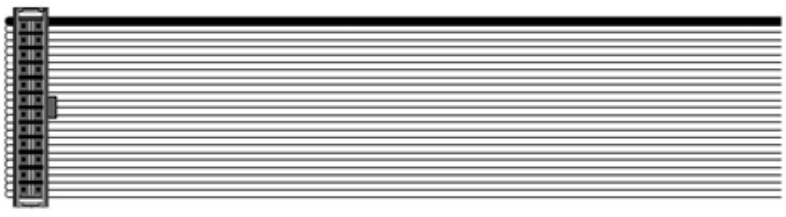
PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	5V		-	-	
2	SPDIF-OUT		-	-	
3	GND	PWR	-	-	

7.10 Front Panel Connector (FRONTPNL) (J2)

Note	Pull U/D	Ioh/ Iol	Type	Signal	PIN		Signal	Type	Ioh/ Iol	Pull U/D	Note
	-	-	PWR	USB10/11_5V	1	2	USB10/11_5V	PWR	-	-	
	-	-		USB10-	3	4	USB11-		-	-	
	-	-		USB10+	5	6	USB11+		-	-	
	-	-	PWR	GND	7	8	GND	PWR	-	-	
	-	-	NC	NC	9	10	Headphone-L		-	-	
	-	-	PWR	+5V	11	12	+5V	PWR	-	-	
	-	25/25mA	O	SATA_LED#	13	14	SUS_LED	O	7mA	-	
	-	-	PWR	GND	15	16	PWRBTN_IN#	I		1K1	
	4K7	-	I	RSTIN#	17	18	GND	PWR	-	-	
	-	-	PWR	SB3V3	19	20	Headphone-R		-	-	
	-	-	PWR	AGND	21	22	AGND	PWR	-	-	
	-	-	AI	MIC2-L	23	24	MIC2-R	AI	-	-	

Signal	Description
USB10/11_5V	5V supply for external devices. SB5V is supplied during powerdown to allow wakeup on USB device activity. Protected by resettable 1.1A fuse covering both USB ports.
USB10+/USB10-	Universal Serial Bus Port 10 Differentials: Bus Data/Address/Command Bus.
USB11+/USB11-	Universal Serial Bus Port 11 Differentials: Bus Data/Address/Command Bus.
+5V	Maximum load is 1A or 2A per pin if using IDC connector flat cable or crimp terminals respectively.
SATA_LED#	SATA Activity LED (active low signal). 3V3 output when passive.
SUS_LED	Suspend Mode LED (active high signal). Output 3.3V via 470Ω.
PWRBTN_IN#	Power Button In. Toggle this signal low to start the ATX / BTX PSU and boot the board.
RSTIN#	Reset Input. When pulled low for a minimum 16ms, the reset process will be initiated. The reset process continues even though the Reset Input is kept low.
Headphone	Headphone stereo signals (different audio stereo channel than Front Speaker signals).
MIC2	MIC2 is second stereo microphone input.
SB3V3	Standby 3.3V voltage.
AGND	Analogue Ground for Audio.

Available cable kit:



PN 821042 Cable Front Panel Open-End, 300 mm

7.11 Feature Connector (Feature) (J1)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
2	2M/	-	I	CASE_OPEN#	1	2	SMBC		/4mA	10K/	1
	-	25/25mA	O	S5#	3	4	SMBD		/4mA	10K/	1
	-	25/25mA	O	PWR_OK	5	6	EXT_BAT	PWR	-	-	
5	-		O	FAN3OUT	7	8	FAN3IN	I	-	-	5
	-	-	PWR	SB3V3	9	10	SB5V	PWR	-	-	
	-		IOT	GPIO0	11	12	GPIO1	IOT		-	
	-		IOT	GPIO2	13	14	GPIO3	IOT		-	
	-		IOT	GPIO4	15	16	GPIO5	IOT		-	
	-		IOT	GPIO6	17	18	GPIO7	IOT		-	
	-	-	PWR	GND	19	20	GND	PWR	-	-	
	-		I	GPIO8	21	22	GPIO9	I		-	
	-		I	GPIO10	23	24	GPIO11	I		-	
	-		I	GPIO12	25	26	GPIO13	IOT		-	
4	-		IOT	GPIO14	27	28	GPIO15	IOT		-	
4	-		IOT	GPIO16	29	30	GPIO17	IOT		-	
	-	-	PWR	GND	31	32	GND	PWR	-	-	
	-	8/8mA	O	EGCLK	33	34	EGCS#	O	8/8mA	-	
	-	8/8mA		EGAD	35	36	TMA0	O			
	-		PWR	+12V	37	38	GND	PWR	-	-	
4	-		O	FAN4OUT	39	40	FAN4IN	I	-	-	4
	-	-	PWR	GND	41	42	GND	PWR	-	-	
	-	-	PWR	GND	43	44	S3#	O	25/25mA	-	

Notes: 1. Pull-up to +3V3Dual (+3V3 or SB3V3). **2.** Pull-up to on-board Battery. **3.** Pull-up to +3V3. **4.** Not Available. 5. Not available on mITX, Shared with onboard FAN2 on Flex.

Signal	Description
CASE_OPEN#	CASE OPEN, used to detect if the system case has been opened. This signal's status is readable, so it may be used like a GPI when the Intruder switch is not required.
SMBC	SMBus Clock signal
SMBD	SMBus Data signal
S3#	S3 sleep mode, active low output, optionally used to deactivate external system.
S5#	S5 sleep mode, active low output, optionally used to deactivate external system.
PWR_OK	PoWeR OK, signal is high if no power failures are detected. (This is not the same as the P_OK signal generated by ATX PSU).
EXT_BAT	(EXTernal BATtery) option for connecting + terminal of an external primary cell battery (2.5 - 3.47 V) (– terminal connected to GND). The external battery is protected against charging and can be used with/without the on-board battery installed.
FAN3OUT	FAN 3 speed control OUTput, 3.3V PWM signal can be used as Fan control voltage.
FAN3IN	FAN3 Input. 0V to +3V3 amplitude Fan 3 tachometer input.
FAN4OUT	FAN 4 speed control OUTput, 3.3V PWM signal can be used as Fan control voltage.
FAN4IN	FAN4 Input. 0V to +3V3 amplitude Fan 3 tachometer input.
SB3V3	Max. load is 0.75A (1.5A < 1 sec.)
SB5V	StandBy +5V supply.

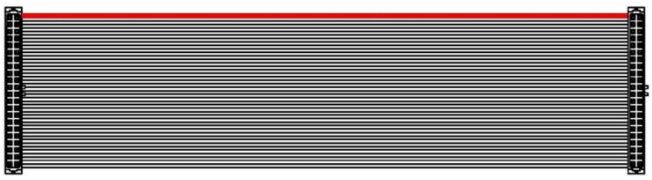
continues

Signal	Description
GPIO0..17	General Purpose Inputs / Output. These Signals may be controlled or monitored through the use of the KT-API-V2 (Application Programming Interface). (GPIO14 and GPIO16 not available, used internally)
EGCLK	Extend GPIO Clock signal
EGAD	Extend GPIO Address Data signal
EGCS#	Extend GPIO Chip Select signal, active low
TMA0	Timer Output
+12V	Max. load is 0.75A (1.5A < 1 sec.)

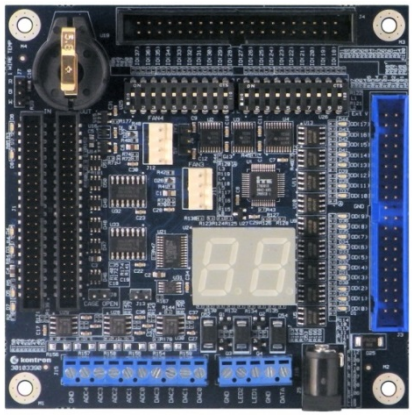
The GPIO's are controlled via the ITE IT8516F Embedded Controller. Each GPIO has 100pF to ground, clamping Diode to 3V3 and has multiplexed functionality. Some pins can be DAC (Digital to Analogue Converter output), PWM (Pulse Width Modulated signal output), ADC (Analogue to Digital Converter input), TMRI (Timer Counter Input), WUI (Wake Up Input), RI (Ring Indicator Input) or some special function.

Signal	IT8516F pin name	Type	Description
GPIO0	DAC0/GPJ0	A0/IOS	
GPIO1	DAC1/GPJ1	A0/IOS	
GPIO2	DAC2/GPJ2	A0/IOS	
GPIO3	DAC3/GPJ3	A0/IOS	
GPIO4	PWM2/GPA2	O8/IOS	
GPIO5	PWM3/GPA3	O8/IOS	
GPIO6	PWM4/GPA4	O8/IOS	
GPIO7	PWM5/GPA5	O8/IOS	
GPIO8	ADC0/GPI0	AI/IS	
GPIO9	ADC1/GPI1	AI/IS	
GPIO10	ADC2/GPI2	AI/IS	
GPIO11	ADC3/GPI3	AI/IS	
GPIO12	ADC4/WUI28/GPI4	AI/IS/IS	
GPIO13	RI1#/WUI0/GPD0	IS/IS/IOS	
GPIO14	RI2#/WUI1/GPD1	IS/IS/IOS	not available (used internally)
GPIO15	TMRI0/WUI2/GPC4	IS/IS/IOS	
GPIO16	TMRI1/WUI3/GPC6	IS/IS/IOS	not available (used internally)
GPIO17	L80HLAT/BA0/WUI24/GPE0	O4/O4/IS/IOS	

Available cable kit and Break-Out-Board:



PN 1052-5885 Cable, Feature 44pol 1 to1, 300mm

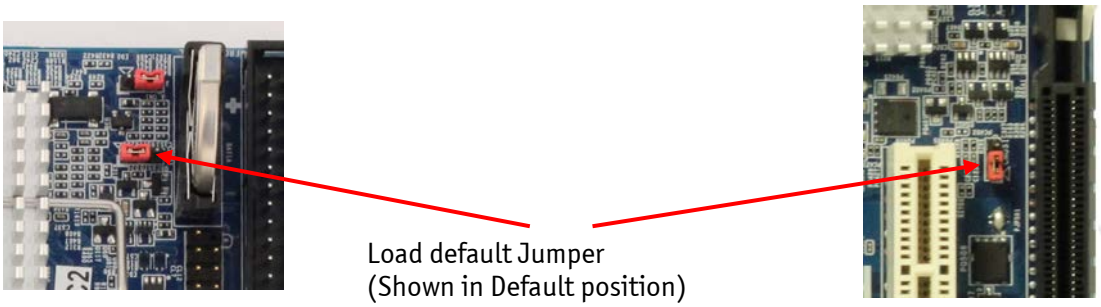


PN 820978 Feature BOB (Break-Out-Board)

7.12 "Load Default BIOS Settings" (Load default) (CMOS)

The "Load Default BIOS Settings" Jumper (J5) can be used to recover from incorrect BIOS settings. As an example, incorrect BIOS setting which causes the attached display not to turn on can be erased by this Jumper.

The Jumper has 3 positions: Pin 1-2, Pin2-3 (default position) and not mounted.



mITX Flex

Warning Don't leave the jumper in position 2-3, otherwise if power is disconnected, the battery will fully deplete within a few weeks.

To **Load Default BIOS Settings**, inclusive erasing password and RTC:

1. Turn off power completely (no SB5V).
2. Remove the Jumper completely from CMOS1.
3. Insert jumper into position 2-3 (Clear CMOS data).
4. Wait for 10 sec.
5. Move the Jumper back to position 1-2 (default position).
6. Turn on power (use the Power On Button if required to boot).
7. Motherboard beeps number of times.
8. CMOS data lost message are shown.
9. Reboot and enter BIOS setup menu and select new settings.

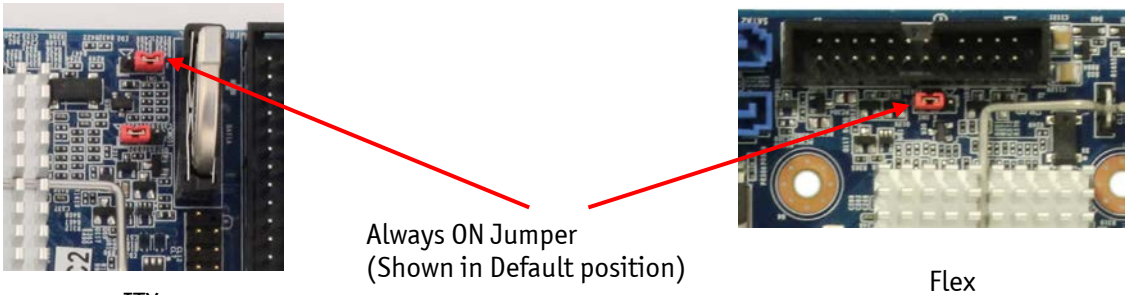
Motherboard might automatically reboot a few times. Wait until booting is completed.

CMOS1		Description
pin1-2	pin2-3	
X	-	Default position
-	X	Load Default BIOS Settings exclusive erasing Password
-	-	No function. Note: may load default BIOS settings after several minutes

7.13 "Always On" (Always On) (A_ON)

The "Always On" can be used to implement hardware controlled Always ON by jumper. When "Always On" is selected, then the board will power up automatically when power is connected.

The board can still be shut down by PWRBTN_IN# (power button in) activation (via Front Panel connector).



mITX

Flex

Always On		Description
pin1-2	pin2-3	
X	-	Always On selection
-	X	Default position
-	-	No function. Note: may load default BIOS settings after several minutes

7.14 SPI Connector (SPI_HEAD)

The SPI Connector is normally not used. If however a SPI BIOS is connected via the SPI Connector then the board will attempt to boot from it.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
1	-			CLK	1	2	SB3V3	PWR	-	-	
	-		I	CS0#	3	4	ADDIN	IO		/10K	
	10K/		-	NC	5	6	NC	-	-	-	
	10K/		IO	MOSI	7	8	ISOLATE#	IO		100K	
	-		IO	MISO	9	10	GND	PWR	-	-	
	1K		IO	SPI_IO2_#WP	11	12	SPI_IO3_#HOLD	IO		1K	

Signal	Description
CLK	Serial Clock
SB3V3	3.3V Standby Voltage power line. Normally output power, but when Motherboard is turned off then the on-board SPI Flash can be 3.3V power sourced via this pin.
CS0#	CS0# Chip Select 0, active low.
ADDIN	ADDIN input signal must be NC.
MOSI	Master Output, Slave Input.
ISOLATE#	The ISOLATE# input, active low, is normally NC, but must be connected to GND when programming the SPI flash. Power Supply to the Motherboard must be turned off when loading SPI flash. The pull up resistor is connected via diode to 5VSB.
MISO	Master Input, Slave Output
SPI_IO2_#WP	SPI Data I/O: A bidirectional signal used to support Dual IO Fast Read, Quad IO Fast Read and Quad Output Fast Read modes. The signal is not used in Dual Output Fast Read mode.
SPI_IO3_#HOLD	SPI Data I/O: A bidirectional signal used to support Dual IO Fast Read, Quad IO Fast Read and Quad Output Fast Read modes. The signal is not used in Dual Output Fast Read mode.

7.15 LPC Connector (J30)

The LPC connector (Flex board only) is in general unsupported. Only under special circumstances may the LPC interface be of interest.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	LPC CLK	1	2	GND				
	-	-	PWR	LPC FRAME#	3		KEY				
				LPC RST#	5	6	+5V				
				LPC AD3	7	8	LPC AD2				
				+3V3	9	10	LPC AD1				
				LPC AD0	11	12	GND				
				SMB_CLK	13	14	SMB_DATA				
				SB3V3	15	16	LPC SERIRQ				
				GND	17	18	CLKRUN#				
				SUS_STAT#	19	20	TPM_DRQ#0				

7.16 XDP_CPU (Debug Port for CPU) (XDP_CPU)

The XDP_CPU (Intel Debug Port for CPU) connector is not mounted and not supported. XDP connector layout (pads) is located on the backside of PCB and is prepared for the Samtec BSH-030-01-F-D-A-TR.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
			PWR	GND	1	2	GND	PWR			
				REQ	3	4	STB_0_DP				
				RDY	5	6	STB_0_DN				
			PWR	GND	7	8	GND	PWR			
				CFG0	9	10	CFG8				
				CFG1	11	12	CFG9				
			PWR	GND	13	14	GND	PWR			
				CFG2	15	16	CFG10				
				CFG3	17	18	CFG11				
			PWR	GND	19	20	GND	PWR			
				BPM#0	21	22	STB_1_DP				
				BPM#1	23	24	STB_1_DN				
			PWR	GND	25	26	GND	PWR			
				CFG4	27	28	CFG12				
				CFG5	29	30	CFG13				
			PWR	GND	31	32	GND	PWR			
				CFG6	33	34	CFG14				
				CFG7	35	36	CFG15				
			PWR	GND	37	38	GND	PWR			
				PWRGD	39	40	ITP_CLKP				
				SW_ON_N	41	42	ITP_CLKN				
			PWR	CPU_VCCIO	43	44	CPU_VCCIO	PWR			
				PWR_DEBUG	45	46	RESET#				
				CPU_HOOK3	47	48	DBR#				
			PWR	GND	49	50	GND	PWR			
				SMB_DAT	51	52	TDO				
				SMB_CLK	53	54	TRST#				
				NC	55	56	TDI				
				TCK	57	58	TMS				
			PWR	GND	59	60	XDP_PRESENT#				

7.17 XDP_PCH (Debug Port for Chipset) (XDP_PCH)

The XDP_PCH (Intel Debug Port for Chipset) connector is not mounted and not supported. XDP_PCH connector layout (pads) is located on the backside of PCB (below J35 connector on mITX version) and is prepared for the Samtec BSH-030-01-F-D-A-TR.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
			PWR	GND	1	2	GND	PWR			
				NC	3	4	EC_WRST#				
				NC	5	6	2x4_PWR_DETECT				
			PWR	GND	7	8	GND	PWR			
				XDP_0	9	10	SATA0GP				
				XDP_1	11	12	SATA1GP				
			PWR	GND	13	14	GND	PWR			
				XDP_2	15	16	GP36				
				XDP_3	17	18	GP37				
			PWR	GND	19	20	GND	PWR			
				NC	21	22	NC				
				NC	23	24	NC				
			PWR	GND	25	26	GND	PWR			
				XDP_4	27	28	SATA4GP				
				XDP_5	29	30	GP49				
			PWR	GND	31	32	GND	PWR			
				XDP_6	33	34	GPIO18				
				XDP_7	35	36	SMI_N				
			PWR	GND	37	38	GND	PWR			
				PWRGD	39	40	JTAG_VREF				
				HOOK1	41	42	NC				
			PWR	3.3V	43	44	3.3V	PWR			
				NC	45	46	RESET#				
				NC	47	48	HOOK7				
			PWR	GND	49	50	GND	PWR			
				SMB_DAT	51	52	JTAG_TDO				
				SMB_CLK	53	54	JTAG_RST				
				NC	55	56	JTAG_TDI				
				JTAG_TCK	57	58	JTAG_TMS				
			PWR	GND	59	60	GND	PWR			

8 Slot Connectors (PCIe, mPCIe, mSATA, PCI)

8.1 PCIe Connectors

The mITX boards supports one PCIex16 (16-lanes), one miniPCIe and one mSATA in mPCIe slot.

The Flex boards supports one PCIex16 (16-lanes), one PCIex2 (2-lanes) in a x16 slot and one PCIex1 slot.

The **PCIex16** port can be used for external PCI Express cards inclusive graphics card. (On the Flex boards it is located nearest the CPU). Maximum theoretical bandwidth depends on the chipset, Q87 / H81 support up to PCIe 3.0 / PCIe 2.0, so Q87 support 8 Gbps effectively for each lane and direction, 256 Gbps in total for 16 lanes, while the H81 support 4 Gbps effectively for each lane and direction, 128 Gbps in total for 16 lanes.

The **PCIex2** (in a x16 slot) (only on Flex board) can be used for external PCI Express cards inclusive graphics card. It is located fares away from CPU. Maximum theoretical bandwidth is 4 Gbps effectively for each lane and direction, 16 Gbps in total for 2 lanes.

The **PCIex1** (only on Flex board) can be used for external PCI Express cards inclusive graphics card. Maximum theoretical bandwidth is 4 Gbps effectively for each direction, 8 Gbps in total.

One **miniPCIe** (PCIe 2.0) port (mITX boards only) supporting mPCIe cards.

One **miniPCIe** (mSATA) port (mITX boards only) supporting mSATA cards.

miniPCIe slots are equipped with one USB 2.0 port. The USB connected to the mSATA slot do not support WAKE function.

PCI-Express x16 Connector (PCIex16) (SLOT1_16X)

Note	Type	Signal	PIN		Signal	Type	Note
		+12V	B1	A1	NC		
		+12V	B2	A2	+12V		
		+12V	B3	A3	+12V		
		GND	B4	A4	GND		
		SMB_CLK	B5	A5	NC		
		SMB_DATA	B6	A6	NC		
		GND	B7	A7	NC		
		+3V3	B8	A8	NC		
		NC	B9	A9	+3V3		
		SB3V3	B10	A10	+3V3		
		WAKE#	B11	A11	RST#		
		NC	B12	A12	GND		
		GND	B13	A13	PCIE_x16 CLK		
		PEG_TXP[0]	B14	A14	PCIE_x16 CLK#		
		PEG_TXN[0]	B15	A15	GND		
		GND	B16	A16	PEG_RXP[0]		
		CLKREQ	B17	A17	PEG_RXN[0]		
		GND	B18	A18	GND		
		PEG_TXP[1]	B19	A19	NC		
		PEG_TXN[1]	B20	A20	GND		
		GND	B21	A21	PEG_RXP[1]		
		GND	B22	A22	PEG_RXN[1]		

		PEG_TXP[2]	B23	A23	GND		
		PEG_TXN[2]	B24	A24	GND		
		GND	B25	A25	PEG_RXP[2]		
		GND	B26	A26	PEG_RXN[2]		
		PEG_TXP[3]	B27	A27	GND		
		PEG_TXN[3]	B28	A28	GND		
		GND	B29	A29	PEG_RXP[3]		
		NC	B30	A30	PEG_RXN[3]		
		CLKREQ	B31	A31	GND		
		GND	B32	A32	NC		
		PEG_TXP[4]	B33	A33	NC		
		PEG_TXN[4]	B34	A34	GND		
		GND	B35	A35	PEG_RXP[4]		
		GND	B36	A36	PEG_RXN[4]		
		PEG_TXP[5]	B37	A37	GND		
		PEG_TXN[5]	B38	A38	GND		
		GND	B39	A39	PEG_RXP[5]		
		GND	B40	A40	PEG_RXN[5]		
		PEG_TXP[6]	B41	A41	GND		
		PEG_TXN[6]	B42	A42	GND		
		GND	B43	A43	PEG_RXP[6]		
		GND	B44	A44	PEG_RXN[6]		
		PEG_TXP[7]	B45	A45	GND		
		PEG_TXN[7]	B46	A46	GND		
		GND	B47	A47	PEG_RXP[7]		
		CLKREQ	B48	A48	PEG_RXN[7]		
		GND	B49	A49	GND		
		PEG_TXP[8]	B50	A50	NC		
		PEG_TXN[8]	B51	A51	GND		
		GND	B52	A52	PEG_RXP[8]		
		GND	B53	A53	PEG_RXN[8]		
		PEG_TXP[9]	B54	A54	GND		
		PEG_TXN[9]	B55	A55	GND		
		GND	B56	A56	PEG_RXP[9]		
		GND	B57	A57	PEG_RXN[9]		
		PEG_TXP[10]	B58	A58	GND		
		PEG_TXN[10]	B59	A59	GND		
		GND	B60	A60	PEG_RXP[10]		
		GND	B61	A61	PEG_RXN[10]		
		PEG_TXP[11]	B62	A62	GND		
		PEG_TXN[11]	B63	A63	GND		
		GND	B64	A64	PEG_RXP[11]		
		GND	B65	A65	PEG_RXN[11]		
		PEG_TXP[12]	B66	A66	GND		
		PEG_TXN[12]	B67	A67	GND		
		GND	B68	A68	PEG_RXP[12]		
		GND	B69	A69	PEG_RXN[12]		
		PEG_TXP[13]	B70	A70	GND		
		PEG_TXN[13]	B71	A71	GND		
		GND	B72	A72	PEG_RXP[13]		
		GND	B73	A73	PEG_RXN[13]		
		PEG_TXP[14]	B74	A74	GND		
		PEG_TXN[14]	B75	A75	GND		
		GND	B76	A76	PEG_RXP[14]		
		GND	B77	A77	PEG_RXN[14]		
		PEG_TXP[15]	B78	A78	GND		
		PEG_TXN[15]	B79	A79	GND		
		GND	B80	A80	PEG_RXP[15]		
		CLKREQ	B81	A81	PEG_RXN[15]		
		NC	B82	A82	GND		

PCI-Express x2 Connector (PCIex2) in x16 slot (PCIE2)

(Flex boards only).

Note	Type	Signal	PIN		Signal	Type	Note
		+12V	B1	A1	NC		
		+12V	B2	A2	+12V		
		+12V	B3	A3	+12V		
		GND	B4	A4	GND		
		SMB_CLK	B5	A5	NC		
		SMB_DATA	B6	A6	NC		
		GND	B7	A7	NC		
		+3V3	B8	A8	NC		
		NC	B9	A9	+3V3		
		SB3V3	B10	A10	+3V3		
		WAKE#	B11	A11	RST#		
		NC	B12	A12	GND		
		GND	B13	A13	PCIE_x16 CLK		
		PEG_TXP[0]	B14	A14	PCIE_x16 CLK#		
		PEG_TXN[0]	B15	A15	GND		
		GND	B16	A16	PEG_RXP[0]		
		CLKREQ	B17	A17	PEG_RXN[0]		
		GND	B18	A18	GND		
		PEG_TXP[1]	B19	A19	NC		
		PEG_TXN[1]	B20	A20	GND		
		GND	B21	A21	PEG_RXP[1]		
		GND	B22	A22	PEG_RXN[1]		
			B23	A23	GND		
			B24	A24	GND		
		GND	B25	A25			
		GND	B26	A26			
			B27	A27	GND		
			B28	A28	GND		
		GND	B29	A29			
		NC	B30	A30			
		CLKREQ	B31	A31	GND		
		GND	B32	A32	NC		
			B33	A33	NC		
			B34	A34	GND		
		GND	B35	A35			
		GND	B36	A36			
			B37	A37	GND		
			B38	A38	GND		
		GND	B39	A39			
		GND	B40	A40			
			B41	A41	GND		
			B42	A42	GND		
		GND	B43	A43			
		GND	B44	A44			
			B45	A45	GND		
			B46	A46	GND		
		GND	B47	A47			
		CLKREQ	B48	A48			
		GND	B49	A49	GND		

			B50	A50	NC		
			B51	A51	GND		
		GND	B52	A52			
		GND	B53	A53			
			B54	A54	GND		
			B55	A55	GND		
		GND	B56	A56			
		GND	B57	A57			
			B58	A58	GND		
			B59	A59	GND		
		GND	B60	A60			
		GND	B61	A61			
			B62	A62	GND		
			B63	A63	GND		
		GND	B64	A64			
		GND	B65	A65			
			B66	A66	GND		
			B67	A67	GND		
		GND	B68	A68			
		GND	B69	A69			
			B70	A70	GND		
			B71	A71	GND		
		GND	B72	A72			
		GND	B73	A73			
			B74	A74	GND		
			B75	A75	GND		
		GND	B76	A76			
		GND	B77	A77			
			B78	A78	GND		
			B79	A79	GND		
		GND	B80	A80			
		CLKREQ	B81	A81			
		NC	B82	A82	GND		

PCI-Express x1 Connector (PCIex1) (PCIE3)

Only on Flex boards.

Note	Type	Signal	PIN#		Signal	Type	Note
		+12V	B1	A1	NC		
		+12V	B2	A2	+12V		
		+12V	B3	A3	+12V		
		GND	B4	A4	GND		
		SMB_CLK	B5	A5	NC		
		SMB_DATA	B6	A6	NC		
		GND	B7	A7	NC		
		+3V3	B8	A8	NC		
		NC	B9	A9	+3V3		
		SB3V3	B10	A10	+3V3		
		WAKE#	B11	A11	RST#		
		NC	B12	A12	GND		
		GND	B13	A13	PCIE CLK		
		PCIE_TXP	B14	A14	PCIE CLK#		
		PCIE_TXN	B15	A15	GND		
		GND	B16	A16	PCIE_RXP		
		NC	B17	A17	PCIE_RXN		
		GND	B18	A18	GND		

miniPCI-Express mPCIe (MPCIE)

(mITX boards only).

The miniPCIe port supports mPCIe and USB 2.0 cards (not mSATA).

Note	Type	Signal	PIN		Signal	Type	Note
		WAKE#	1	2	+3V3	PWR	
	NC	NC	3	4	GND	PWR	
	NC	NC	5	6	+1.5V	PWR	
1		CLKREQ#	7	8	NC	NC	
	PWR	GND	9	10	NC	NC	
		PCIE_mini CLK#	11	12	NC	NC	
		PCIE_mini CLK	13	14	NC	NC	
	PWR	GND	15	16	NC	NC	
	NC	NC	17	18	GND	PWR	
	NC	NC	19	20	W_Disable#		2
	PWR	GND	21	22	RST#		
		PCIE_RXN	23	24	+3V3 Dual	PWR	
		PCIE_RXP	25	26	GND	PWR	
	PWR	GND	27	28	+1.5V	PWR	
	PWR	GND	29	30	SMB_CLK		
		PCIE_TXN	31	32	SMB_DATA		
		PCIE_TXP	33	34	GND	PWR	
	PWR	GND	35	36	U_USB8N	IO	
	PWR	GND	37	38	U_USB8P	IO	
	PWR	+3V3 Dual	39	40	GND	PWR	
	PWR	+3V3 Dual	41	42	NC	NC	
	PWR	GND	43	44	NC	NC	
		CLK_MPCIE	45	46	NC	NC	
		DATA_MPCIE	47	48	+1.5V	PWR	
		RST_MPCIE#	49	50	GND	PWR	
3		SEL_MSATA	51	52	+3V3 Dual	PWR	

Note 1: 10K ohm pull-up to 3V3.
Note 2: 2K2 ohm pull-up to 3V3 Dual.
Note 3: 100K ohm pull-up to 1V8 (S0 mode)

8.2 mSATA (MSATA)

(mITX boards only).

The mSATA port (in mPCIe express connector) supports mSATA and USB 2.0 cards (not PCIe cards).

Note	Type	Signal	PIN		Signal	Type	Note
		WAKE#	1	2	+3V3	PWR	
	NC	NC	3	4	GND	PWR	
	NC	NC	5	6	+1.5V	PWR	
1		CLKREQ#	7	8	NC	NC	
	PWR	GND	9	10	NC	NC	
		PCIE_mini CLK#	11	12	NC	NC	
		PCIE_mini CLK	13	14	NC	NC	
	PWR	GND	15	16	NC	NC	
	NC	NC	17	18	GND	PWR	
	NC	NC	19	20	W_Disable#		2
	PWR	GND	21	22	RST#		
		PCIE_RXN	23	24	+3V3 Dual	PWR	
		PCIE_RXP	25	26	GND	PWR	
	PWR	GND	27	28	+1.5V	PWR	
	PWR	GND	29	30	SMB_CLK		
		PCIE_TXN	31	32	SMB_DATA		
		PCIE_TXP	33	34	GND	PWR	
	PWR	GND	35	36	U_USB9N	IO	
	NC	NC	37	38	U_USB9P	IO	
	NC	NC	39	40	GND	PWR	
	NC	NC	41	42	NC	NC	
	NC	NC	43	44	NC	NC	
	NC	NC	45	46	NC	NC	
	NC	NC	47	48	+1.5V	PWR	
	NC	NC	49	50	GND	PWR	
	NC	NC	51	52	+3V3	PWR	

Note 1: 10K ohm pull-up to 3V3 Dual.
Note 2: 2K2 ohm pull-up to 3V3 Dual.

8.3 PCI Slot Connector

Flex board only.

Note	Type	Signal	Terminal S	Terminal C	Signal	Type	Note
	PWR	-12V	F01	E01	TRST#	O	
	O	TCK	F02	E02	+12V	PWR	
	PWR	GND	F03	E03	TMS	O	
NC	I	TDO	F04	E04	TDI	O	
	PWR	+5V	F05	E05	+5V	PWR	
	PWR	+5V	F06	E06	INTA#	I	
	I	INTB#	F07	E07	INTC#	I	
	I	INTD#	F08	E08	+5V	PWR	
NC	-	-	F09	E09	-	-	NC
NC	-	-	F10	E10	+5V (I/O)	PWR	
NC	-	-	F11	E11	-	-	NC
	PWR	GND	F12	E12	GND	PWR	
	PWR	GND	F13	E13	GND	PWR	
NC	-	-	F14	E14	GNT3#	OT	
	PWR	GND	F15	E15	RST#	O	
	O	CLKB	F16	E16	+5V (I/O)	PWR	
	PWR	GND	F17	E17	GNT0#	OT	
	I	REQ0#	F18	E18	GND	PWR	
	PWR	+5V (I/O)	F19	E19	PME#	I	
	IOT	AD31	F20	E20	AD30	IOT	
	IOT	AD29	F21	E21	+3.3V	PWR	
	PWR	GND	F22	E22	AD28	IOT	
	IOT	AD27	F23	E23	AD26	IOT	
	IOT	AD25	F24	E24	GND	PWR	
	PWR	+3.3V	F25	E25	AD24	IOT	
	IOT	C/BE3#	F26	E26	GNT1#	OT	
	IOT	AD23	F27	E27	+3.3V	PWR	
	PWR	GND	F28	E28	AD22	IOT	
	IOT	AD21	F29	E29	AD20	IOT	
	IOT	AD19	F30	E30	GND	PWR	
	PWR	+3.3V	F31	E31	AD18	IOT	
	IOT	AD17	F32	E32	AD16	IOT	
	IOT	C/BE2#	F33	E33	+3.3V	PWR	
	PWR	GND	F34	E34	FRAME#	IOT	
	IOT	IRDY#	F35	E35	GND	PWR	
	PWR	+3.3V	F36	E36	TRDY#	IOT	
	IOT	DEVSEL#	F37	E37	GND	PWR	
	PWR	GND	F38	E38	STOP#	IOT	
	IOT	LOCK#	F39	E39	+3.3V	PWR	
	IOT	PERR#	F40	E40	SDONE	IO	
	PWR	+3.3V	F41	E41	SB0#	IO	
	IOC	SERR#	F42	E42	GND	PWR	
	PWR	+3.3V	F43	E43	PAR	IOT	
	IOT	C/BE1#	F44	E44	AD15	IOT	
	IOT	AD14	F45	E45	+3.3V	PWR	
	PWR	GND	F46	E46	AD13	IOT	
	IOT	AD12	F47	E47	AD11	IOT	
	IOT	AD10	F48	E48	GND	PWR	
	PWR	GND	F49	E49	AD09	IOT	
SOLDER SIDE					**COMPONENT SIDE**		
	IOT	AD08	F52	E52	C/BE0#	IOT	
	IOT	AD07	F53	E53	+3.3V	PWR	
	PWR	+3.3V	F54	E54	AD06	IOT	
	IOT	AD05	F55	E55	AD04	IOT	
	IOT	AD03	F56	F56	GND	PWR	
	PWR	GND	F57	E57	AD02	IOT	
	IOT	AD01	F58	E58	AD00	IOT	
	PWR	+5V (I/O)	F59	E59	+5V (I/O)	PWR	
	IOT	ACK64#	F60	E60	REQ64#	IOT	
	PWR	+5V	F61	E61	+5V	PWR	
	PWR	+5V	F62	E62	+5V	PWR	

Signal Description – PCI Slot Connector

SYSTEM PINS	
CLK	Clock provides timing for all transactions on PCI and is an input to every PCI device. All other PCI signals, except RST#, INTA#, INTB#, INTC#, and INTD#, are sampled on the risingedge of CLK and all other timing parameters are defined with respect to this edge. PCI operates at 33MHz.
PME#	Power Management Event interrupt signal. Wake up signal.
RST#	Reset is used to bring PCI-specific registers, sequencers, and signals to a consistent state. What effect RST# has on a device beyond the PCI sequencer is beyond the scope of this specification, except for reset states of required PCI configuration registers. Anytime RST# is asserted, all PCI output signals must be driven to their benign state. In general, this means they must be asynchronously tri-stated. SERR# (open drain) is floated. REQ# and GNT# must both be tri-stated (they cannot be driven low or high during reset). To prevent AD, C/BE#, and PAR signals from floating during reset, the central resource may drive these lines during reset (bus parking) but only to a logic low level–they may not be driven high. RST# may be asynchronous to CLK when asserted or deasserted. Although asynchronous, deassertion is guaranteed to be a clean, bounce-free edge. Except for configuration accesses, only devices that are required to boot the system will respond after reset.
ADDRESS AND DATA	
AD[31::00]	Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. The address phase is the clock cycle in which FRAME# is asserted. During the address phase AD[31::00] contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory, it is a DWORD address. During data phases AD[07::00] contain the least significant byte (lsb) and AD[31::24] contain the most significant byte (msb). Write data is stable and valid when IRDY# is asserted and read data is stable and valid when TRDY# is asserted. Data is transferred during those clocks where both IRDY# and TRDY# are asserted.
C/BE[3::0]#	Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3::0]# define the bus command. During the data phase C/BE[3::0]# are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/BE[0]# applies to byte 0 (lsb) and C/BE[3]# applies to byte 3 (msb).
PAR	Parity is even parity across AD[31::00] and C/BE[3::0]#. Parity generation is required by all PCI agents. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. (PAR has the same timing as AD[31::00], but it is delayed by one clock.) The master drives PAR for address and write data phases; the target drives PAR for read data phases.
INTERFACE CONTROL PINS	
FRAME#	Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase or has completed.
IRDY#	Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates that valid data is present on AD[31::00]. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
TRDY#	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD[31::00]. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
STOP#	Stop indicates the current target is requesting the master to stop the current transaction.
LOCK#	Lock indicates an atomic operation that may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed to an address that is not currently locked. A grant to start a transaction on PCI does not guarantee control of LOCK#. Control of LOCK# is obtained under its own protocol in conjunction with GNT#. It is possible for different agents to use PCI while a single master retains ownership of LOCK#. If a device implements Executable Memory, it should also implement LOCK# and guarantee complete access exclusion in that memory. A target of an access that supports LOCK# must provide exclusion to a minimum of 16 bytes (aligned). Host bridges that have system memory behind them should implement LOCK# as a target from the PCI bus point of view and optionally as a master.
IDSEL	Initialization Device Select is used as a chip select during configuration read and write transactions.
DEVSEL#	Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.

ARBITRATION PINS (BUS MASTERS ONLY)	
REQ#	Request indicates to the arbiter that this agent desires use of the bus. This is a point to point signal. Every master has its own REQ# which must be tri-stated while RST# is asserted.
GNT#	Grant indicates to the agent that access to the bus has been granted. This is a point to point signal. Every master has its own GNT# which must be ignored while RST# is asserted. While RST# is asserted, the arbiter must ignore all REQ# lines since they are tri-stated and do not contain a valid request. The arbiter can only perform arbitration after RST# is deasserted. A master must ignore its GNT# while RST# is asserted. REQ# and GNT# are tri-state signals due to power sequencing requirements when 3.3V or 5.0V only add-in boards are used with add-in boards that use a universal I/O buffer.
ERROR REPORTING PINS. The error reporting pins are required by all devices and maybe asserted when enabled	
PERR#	Parity Error is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. The PERR# pin is sustained tri-state and must be driven active by the agent receiving data two clocks following the data when a data parity error is detected. The minimum duration of PERR# is one clock for each data phase that a data parity error is detected. (If sequential data phases each have a data parity error, the PERR# signal will be asserted for more than a single clock.) PERR# must be driven high for one clock before being tri-stated as with all sustained tri-state signals. There are no special conditions when a data parity error may be lost or when reporting of an error may be delayed. An agent cannot report a PERR# until it has claimed the access by asserting DEVSEL# (for a target) and completed a data phase or is the master of the current transaction.
SERR#	System Error is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. If an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required. SERR# is pure open drain and is actively driven for a single PCI clock by the agent reporting the error. The assertion of SERR# is synchronous to the clock and meets the setup and hold times of all bused signals. However, the restoring of SERR# to the deasserted state is accomplished by a weak pullup (same value as used for s/t/s) which is provided by the system designer and not by the 65signaling agent or central resource. This pull-up may take two to three clock periods to fully restore SERR#. The agent that reports SERR#s to the operating system does so anytime SERR# is sampled asserted.
INTERRUPT PINS (OPTIONAL). Interrupts on PCI are optional and defined as “level sensitive,” asserted low (negative true), using open drain output drivers. The assertion and deassertion of INTx# is asynchronous to CLK. A device asserts its INTx# line when requesting attention from its device driver. Once the INTx# signal is asserted, it remains asserted until the device driver clears the pending request. When the request is cleared, the device deasserts its INTx# signal. PCI defines one interrupt line for a single function device and up to four interrupt lines for a multi-function device or connector. For a single function device, only INTA# may be used while the other three interrupt lines have no meaning.	
INTA#	Interrupt A is used to request an interrupt.
INTB#	Interrupt B is used to request an interrupt and only has meaning on a multi-function device.
INTC#	Interrupt C is used to request an interrupt and only has meaning on a multi-function device.
INTD#	Interrupt D is used to request an interrupt and only has meaning on a multi-function device.

KTQ81/Flex & KTH81/Flex PCI IRQ & INT routing

REQ	GNT	IDSEL	INTA	INTB	INTC	INTD
REQ0	GNT0	17	INTA	INTB	INTC	INTD

9 On-board - & Mating Connector Types

The Mating connector(s) / Cable Kits(s) which are fitting the On-board connectors are listed in below table. The highlighted cable kits are included in the "KTQ87 Cable & Driver Kit" PN 826602 / 0200000002. (Different quantity of each cable kit included, depending on the quantity of onboard connectors).

Connector	On-board Connectors		Mating Connectors / Cables	
	Manufacturer	Type no.	Manufacturer	Type no.
CPU_FAN SYS_FAN1 SYS_FAN2	Foxconn	HF0804E-M2	AMP	1375820-4 (4-pole)
	Mighty	21-013-00222-1	AMP	1375820-3 (3-pole)
KBD/MSE	Molex	22-23-2061	Molex	22-01-2065
SATA	FOXCONN	LD1807V-S5BA1DH	Molex	67489-8005
	WINNING	WATM-7DBN4B2B8UW4	Kontron	**PN 821035 (cable)**
ATX24P	CVILUX	CP-01324130	Molex	5557-24R
ATX4P	CHERNGWEEI	CR-W421S-24	Molex	39-01-2045
LVDS	Don Connex	C44-40BSBC1-G	Don Connex	A32-40-C-G-B-1
	SAMTEC	SHF-120-01-F-D-SM-K-TR	Kontron	KT 910000005
	Hon Kon Technology inc	HB12-220-VFS-20	Kontron	KT 821515 (cable)
			Kontron	KT 821155 (cable)
COM1,2	CHERNGWEEI	CHEB254010S	Molex	90635-1103
			Kontron	**PN 821017 (cable)**
			Kontron	PN 821016 (cable)
USB4/5	FOXCONN	HC1105H-P9	Kontron	**PN 821401 (cable)**
USB10/11 *	(FRONTPNL)	-	Kontron	**PN 821401 (cable)**
LPC	PINREX	210-92-10GB04	-	-
Always On Load default	CVILUX	CH11032VA00	-	-
Front Speaker SPDIF	CHERNGWEEI	P101-SGN-060/030-03	-	-
SPI	CHERNGWEEI	P201-SGN-060/030-12	-	-
FRONTPNL	PINREX	510-90-24GB03	Molex	90635-1243
			Kontron	**PN 821042 (cable)**
FEATURE	PINREX	CH74442V100	Don Connex	A05c-44-B-G-A-1-G
			Kontron	**PN 1052-5885 (Cable)**

* USB10/USB11 is located in FRONTPNL connector. Depending on application KT TBD cable kit can be used.

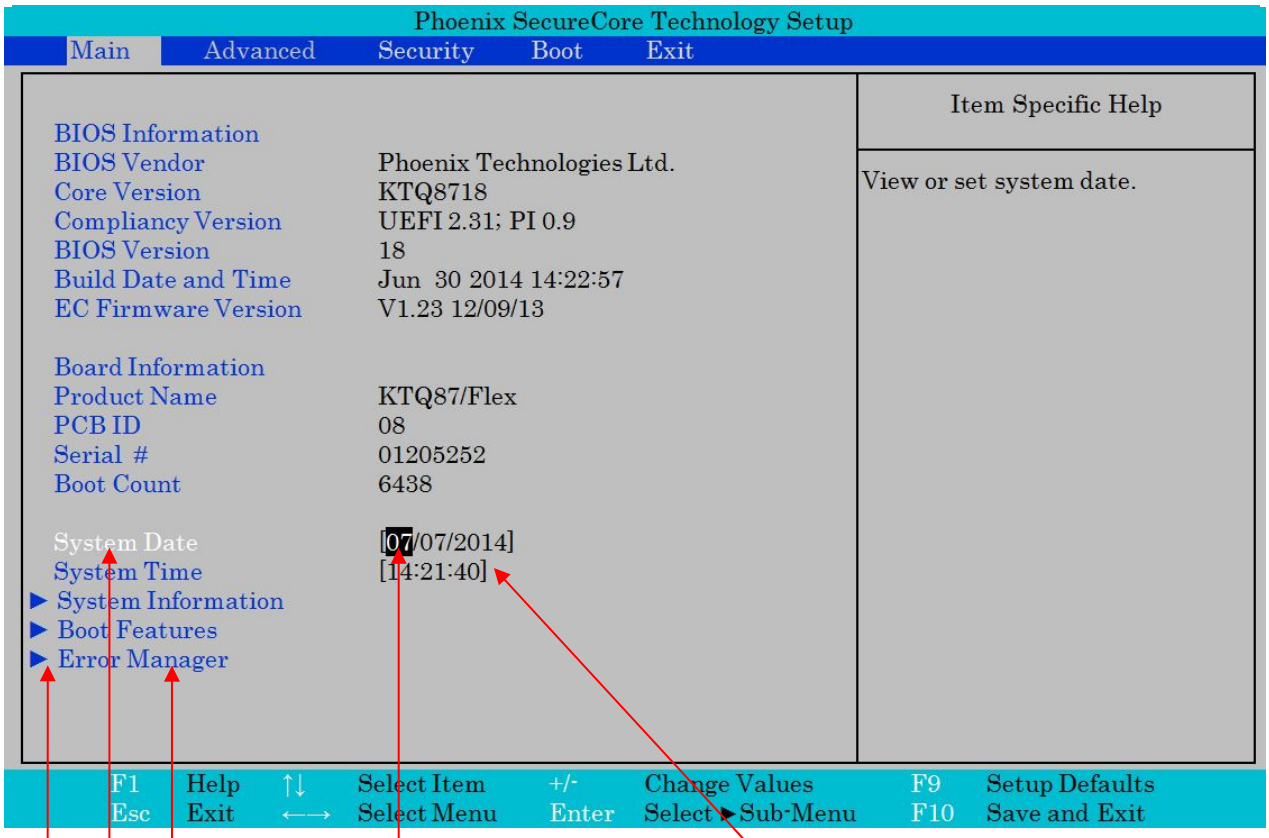
Note: In above table, more than one connector can be listed for each type of on-board connector, if they all have same fit, form and function and are approved by Kontron as an alternative. Please notice that standard connectors like DP, PCI, PCIe, miniPCIe, Audio Jack, Ethernet and USB are not included in the list.

10 BIOS

The BIOS Setup is used to view and configure BIOS settings for the board. The BIOS Setup is accessed by pressing the <Del> -key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins.

The BIOS settings will be loaded automatically when loading "Restore Default" see "Save & Exit" menu. In this Users Guide the default settings are indicated by **bold**. Please notice that "Restore User Defaults" might have different set of default values.

10.1 Main



Sub Menu available.

White text for actual selected function which can be modified.

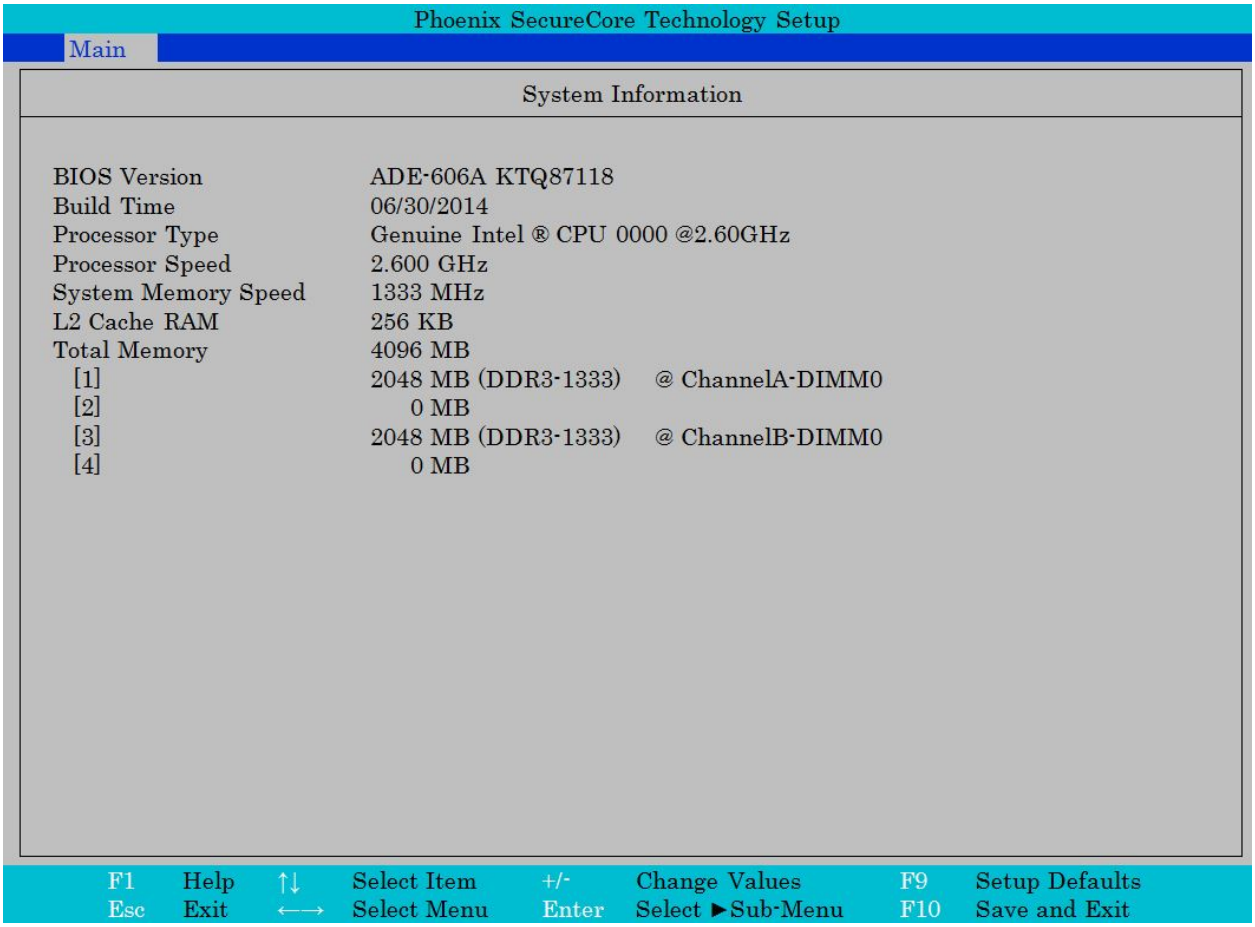
Blue text for functions (not all can be modified).

Black background for actual selection. Black text actual settings.

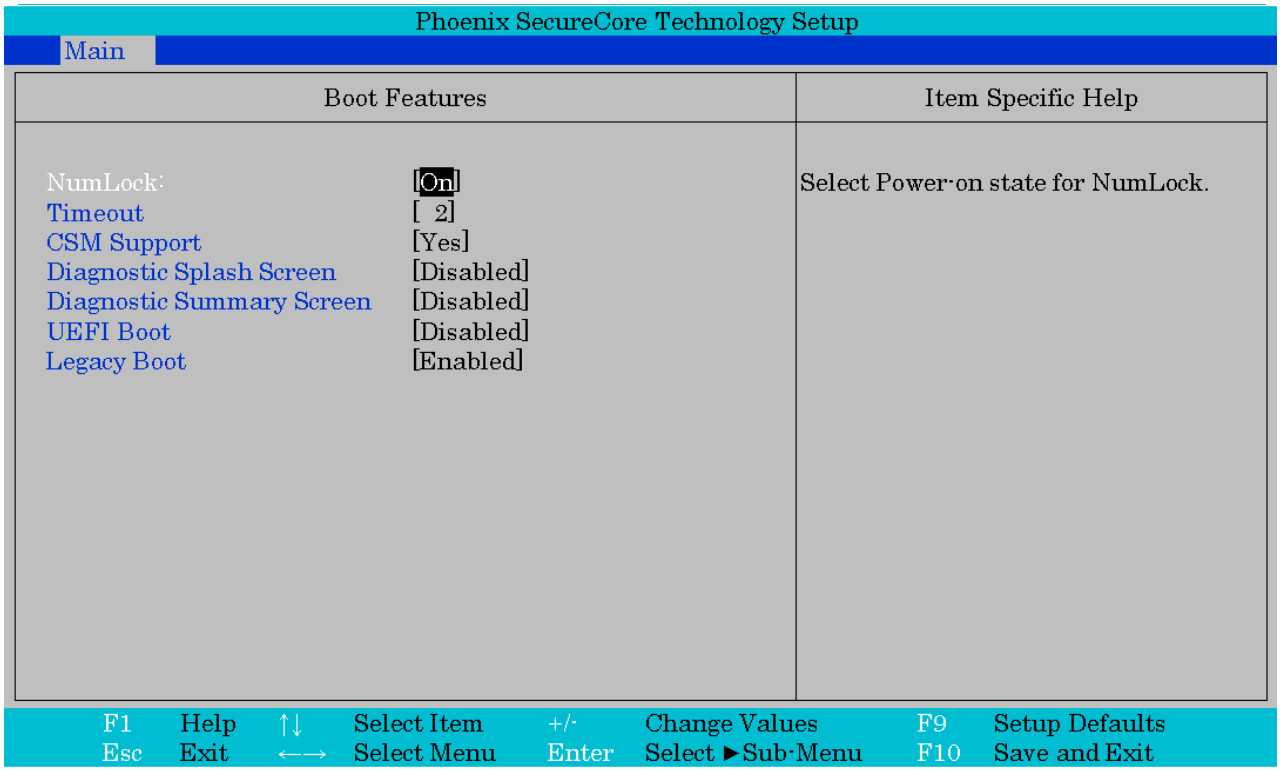
Feature	Options	Description
System Date	MM/DD/YYYY	Set the system date.
System Time	HH:MM:SS	Set the system time.

The following table describes the changeable settings:

System Information



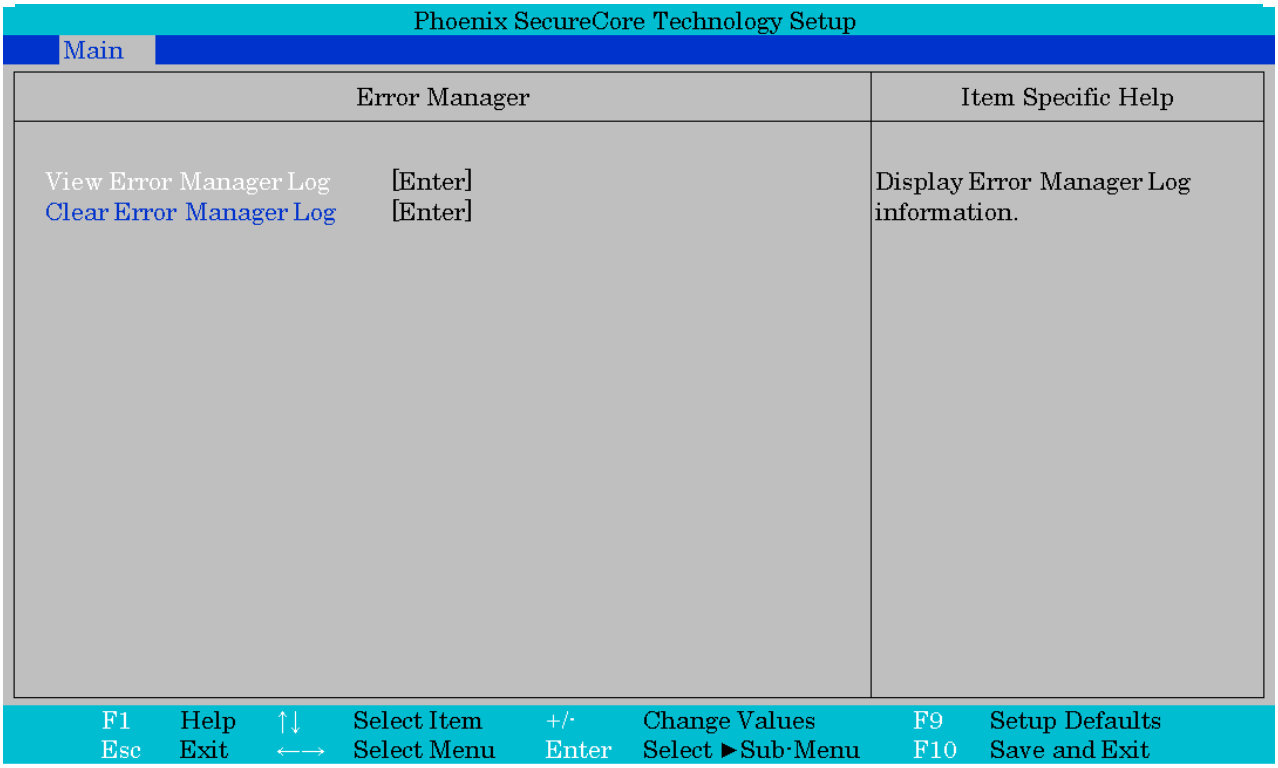
Boot Features



Function	Selection	Description
NumLock:	**On** Off	Select Power-on state for NumLock.
Timeout	2 Note 1	Number of seconds that P.O.S.T will wait for the user input before booting.
CSM Support	No **Yes**	Compatibility Support Module that provides backward compatibility services for legacy BIOS services, like int10/int13, dependent OS.
Diagnostic Splash Screen	**Disabled** Enabled	If you select 'Enabled' the diagnostic splash screen always displays during boot. If you select 'Disabled' the diagnostic splash screen does not display unless you press HOTKEY during boot.
Diagnostic Summary Screen	**Disabled** Enabled	Display the diagnostic summary screen during boot.
UEFI Boot	**Disabled** Enabled	Enable the UEFI boot.
Legacy Boot	Disabled **Enabled**	Enable the Legacy boot.

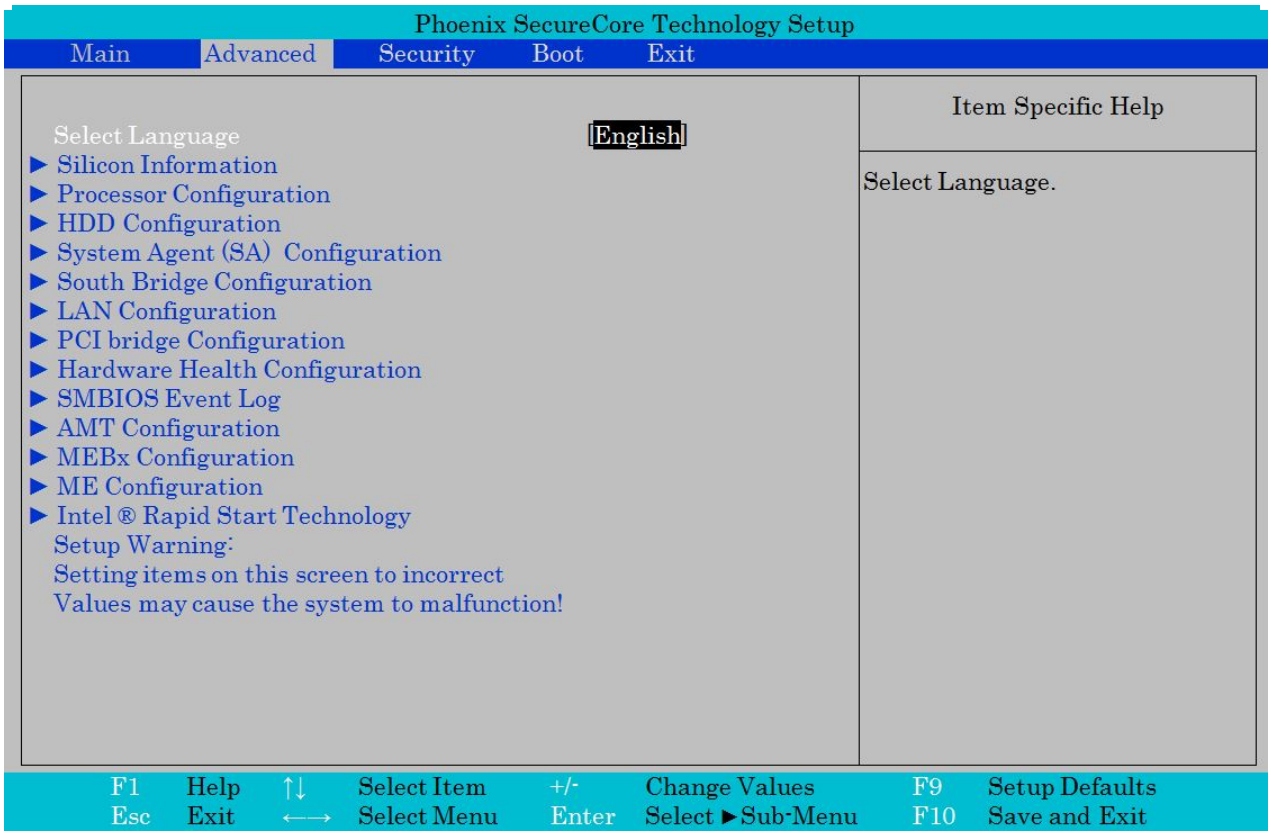
Note 1: Use either digit keys to enter value (0 – 99) or +/- keys to increase/decrease value.

Error Manager



Function	Selection	Description
View Error Manager Log	**Enter**	Display Error Manager Log information.
Clear Error Manager Log	**Enter**	Clear Error Manager Log.

10.2 Advanced

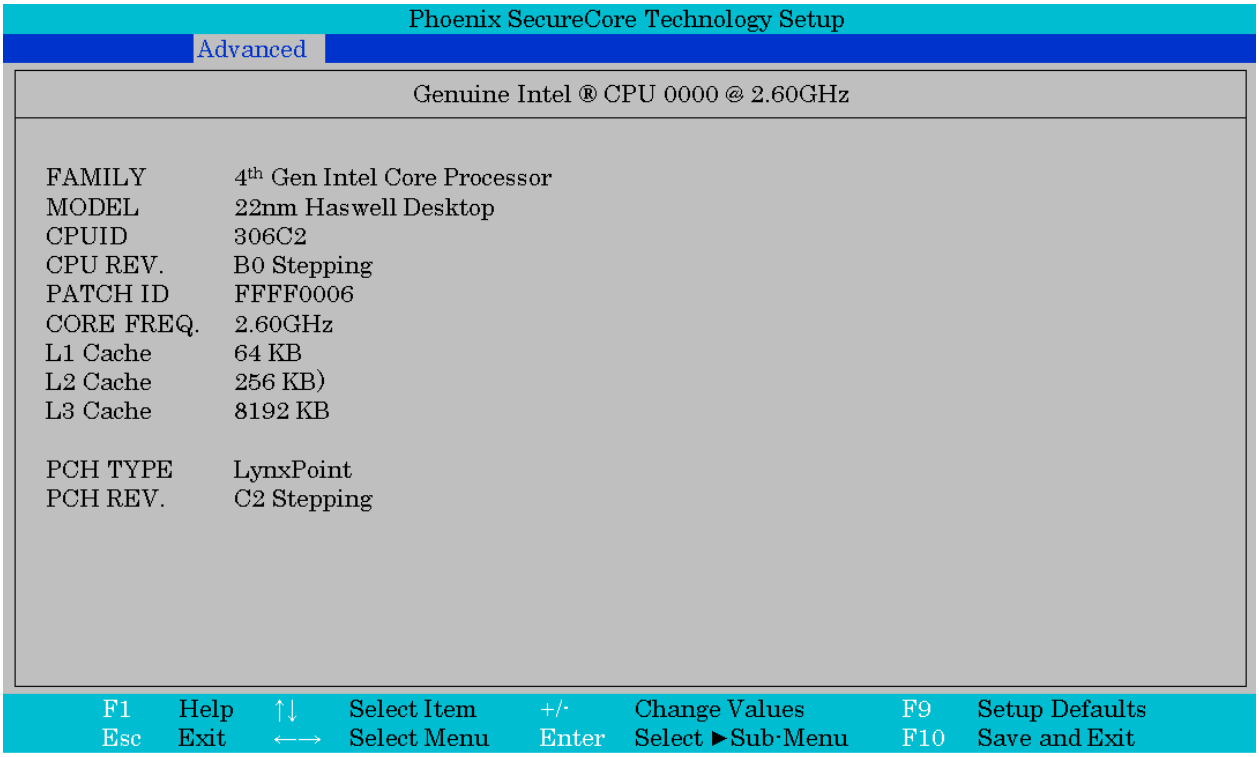


The Advanced (main) menu contains only submenu selections which will be described in more details on the following pages.

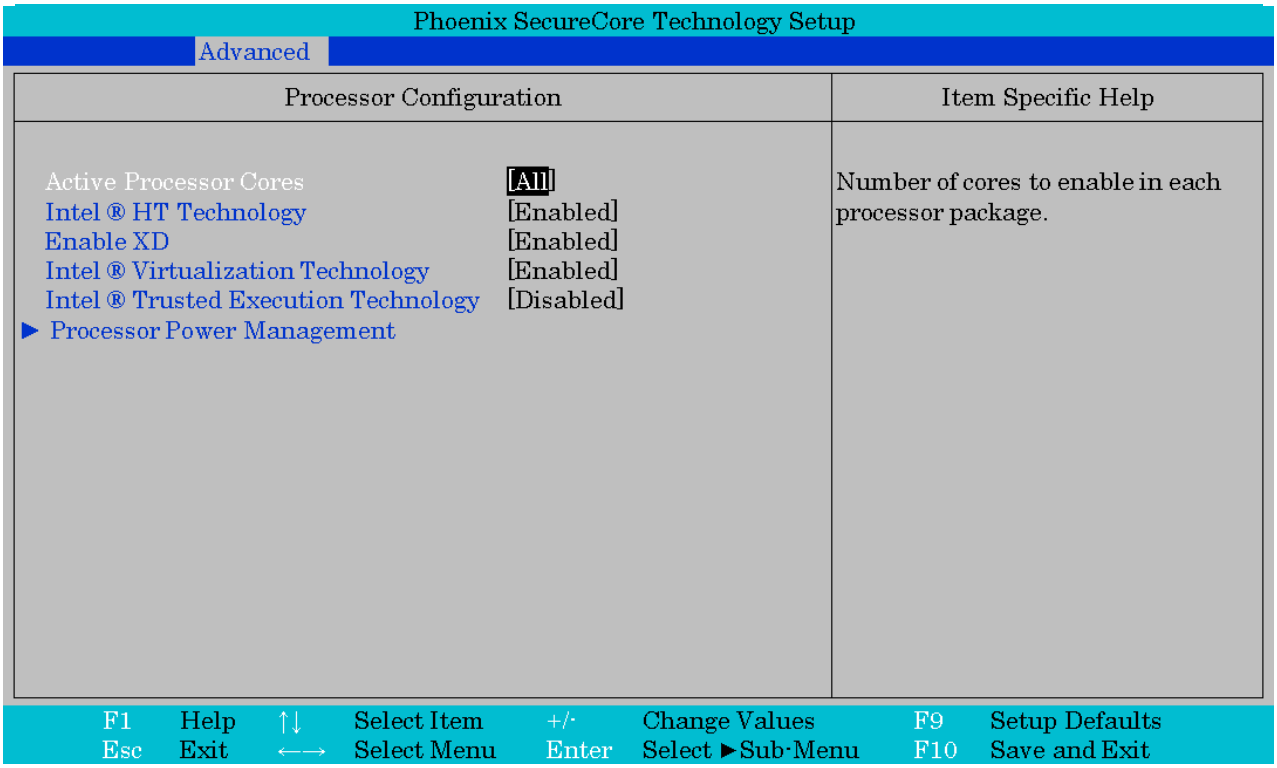
In order to make a selection of a submenu activated the ↑↓ keys until the requested submenu becomes white color, then activate the <Enter>.

Function	Selection	Description
Select Language	**English** Francais Etc.	Select Language.

Silicon Information

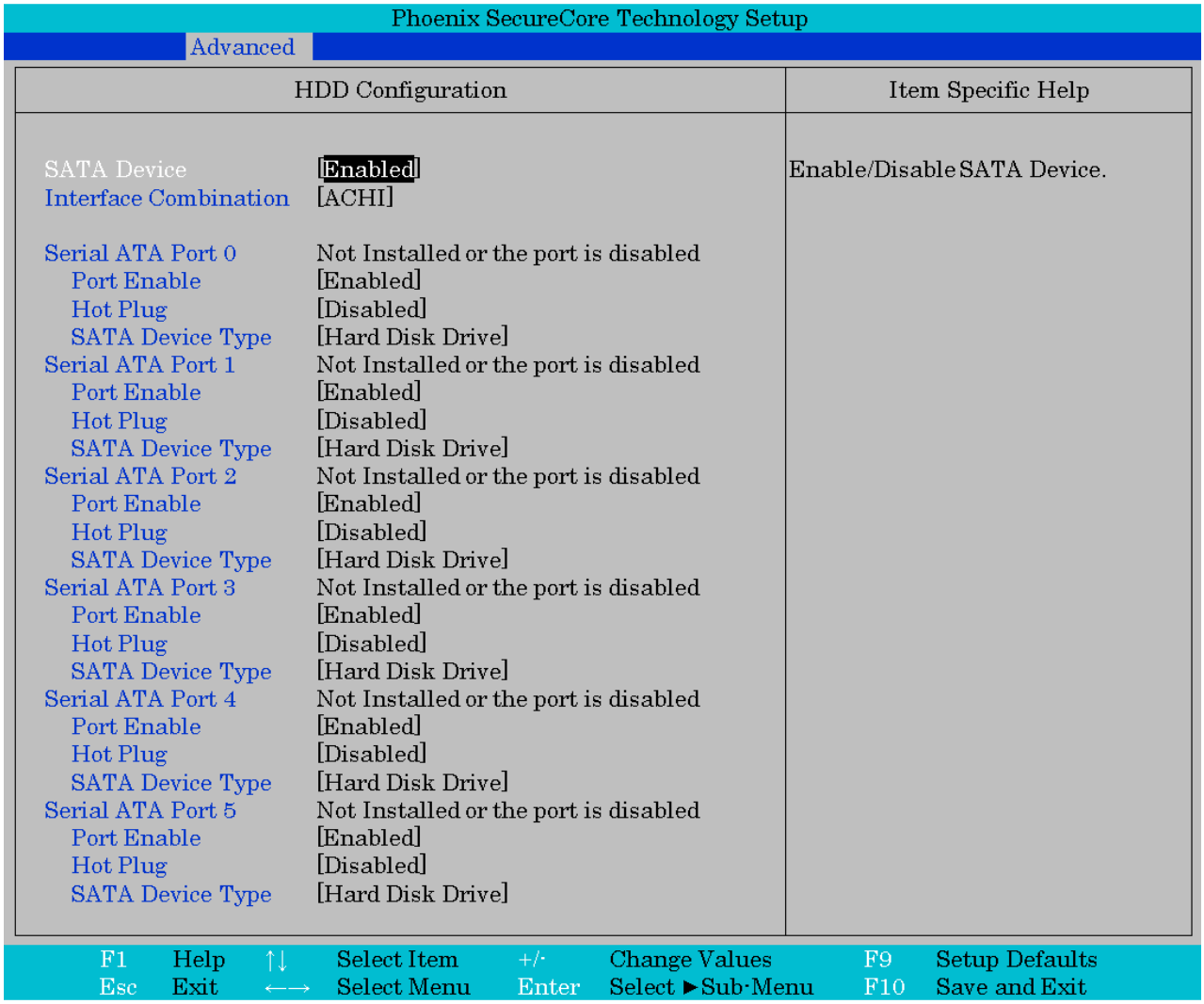


Processor Configuration



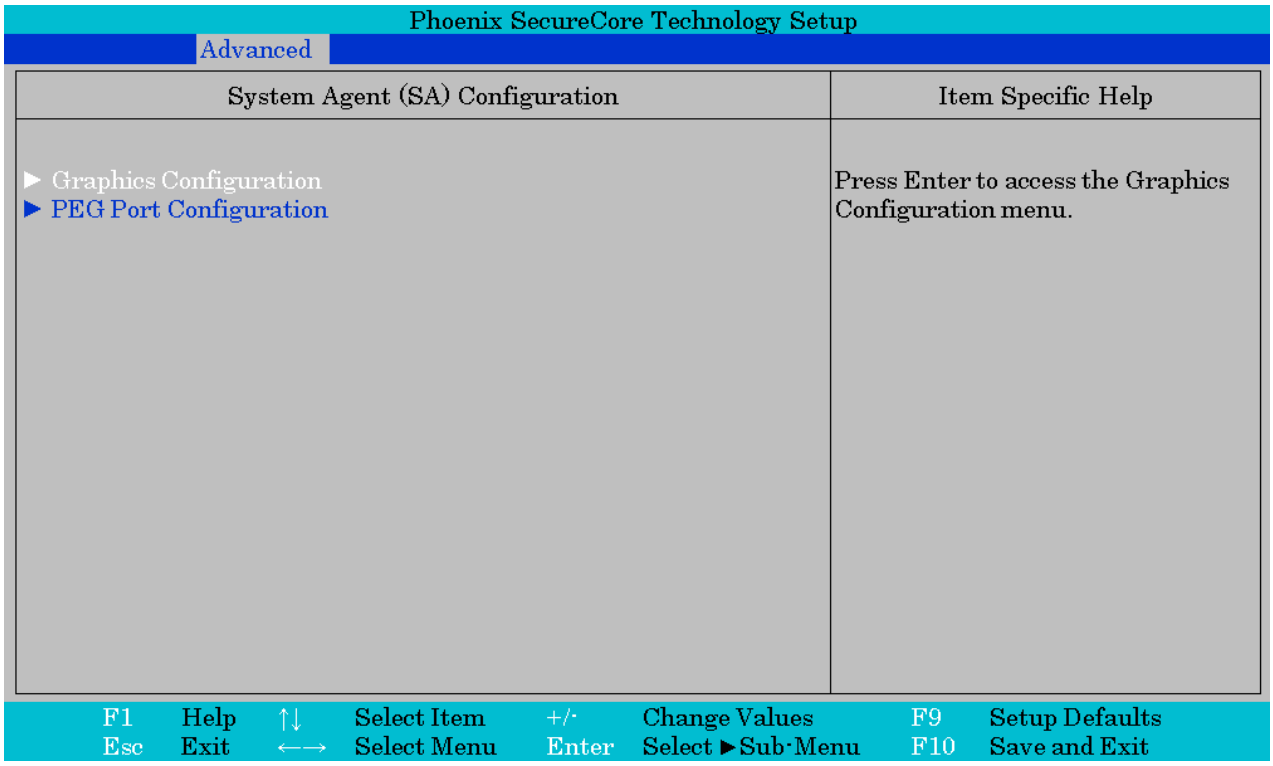
Function	Selection	Description
Active Processor Cores	**All** 1 2 3	Number of cores to enable in each processor package.
Intel ® HT Technology	Disabled **Enabled**	When Disabled only one thread per enabled core is enabled.
Enable XD	Disabled **Enabled**	Enabled Execute Disabled functionality. Also known as Data Execution Prevention (DEP).
Intel ® Virtualization Technology	Disabled **Enabled**	When enabled. A VMM can utilize the additional hardware capabilities.
Intel ® Trusted Execution Technology	**Disabled** Enabled	Enables utilization of additional hardware capabilities provided by Intel ® Trusted Execution Technology. Changes require a full power cycle to take effect.

HDD Configuration

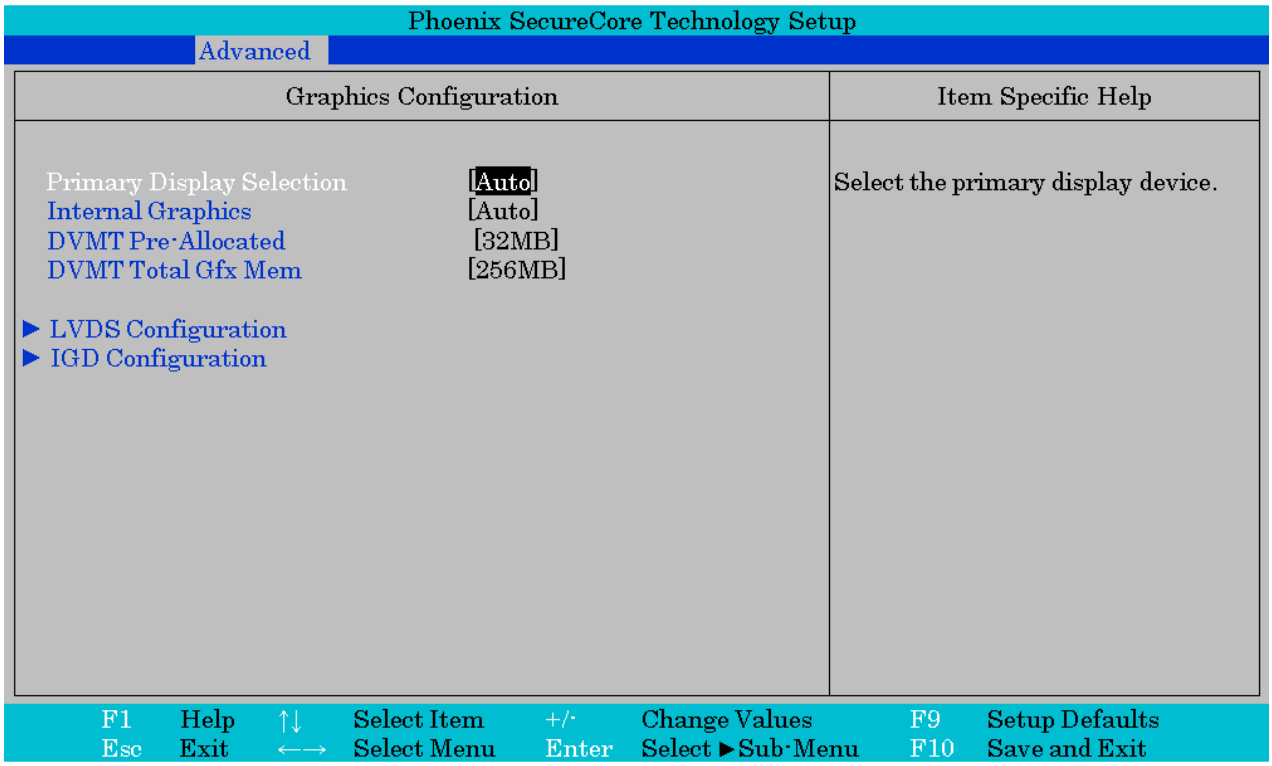


Function	Selection	Description
SATA Device	Disabled **Enabled**	Enable/Disable SATA Device.
Interface Combination	IDE **AHCI** RAID	Select the SATA controllers operation mode.
Serial ATA Port x (x = 0 – 5)	(Device if installed)	
Port Enable	Disabled **Enabled**	Enable/Disable this port.
Hot Plug	**Disabled** Enabled	Designates the port as Hot Pluggable. Note: Requires hardware support.
SATA Device Type	**Hard Disk Drive** Solid State Drive	

System Agent (SA) Configuration

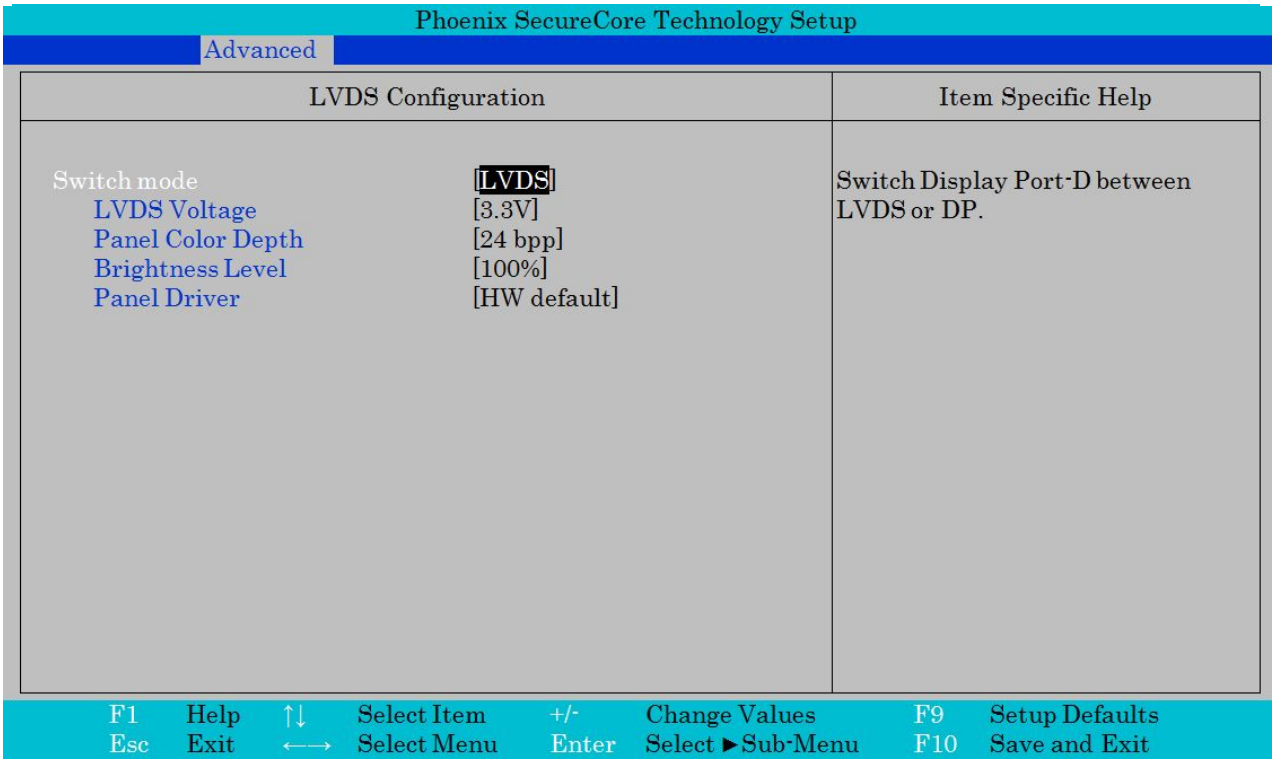


Graphics Configuration



Function	Selection	Description
Primary Display Selection	IGD PEG **Auto**	Select the primary display device.
Internal Graphics	Disabled Enabled **Auto**	Enable/Disable the Internal Graphics Device. This has no effect if external graphics are present.
DVMT Pre-Allocated	**32MB** 64MB 128MB	Select Pre-Allocated Graphics Memory size used by the Internal Graphics Device. This has no effect if external graphics are present.
DVMT Total Gfx Mem	128MB **256MB** MAX	DVMT5.0 DVMT Graphic Memory Size. This has no effect if external graphics are present.

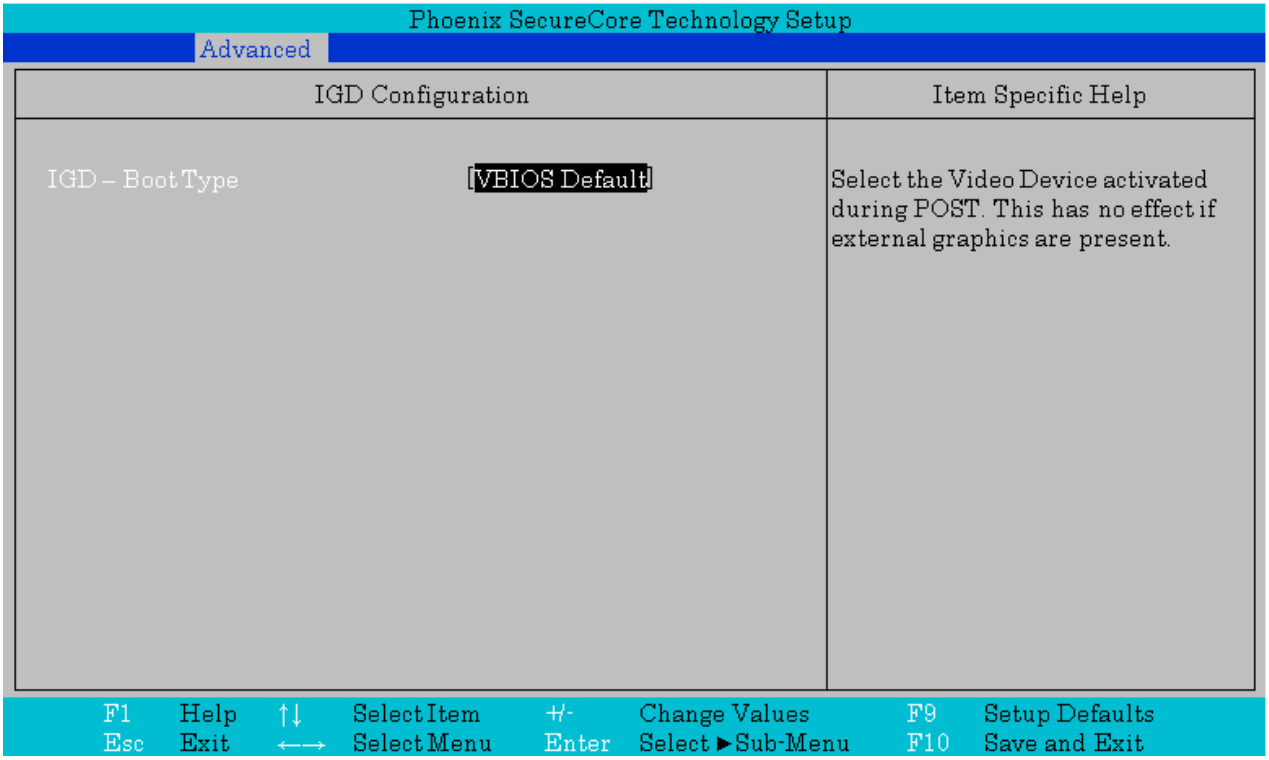
LVDS Configuration



Function		Selection	Description
Switch mode		LVDS **DP**	Switch Display Port-D between LVDS or DP.
LVDS Voltage	Note1	**3.3V** 5V	Select the LVDS Voltage.
Panel Color Depth	Note1	18 bpp **24 bpp**	Select the LVDS Panel Color Depth.
Brightness Level	Note1	0%, 10%, … 100%	Select the LVDS Brightness Level.
Panel Driver	Note1	**HW default** LG 1600x1200 . . . Test 3	Select the Panel (EDID)

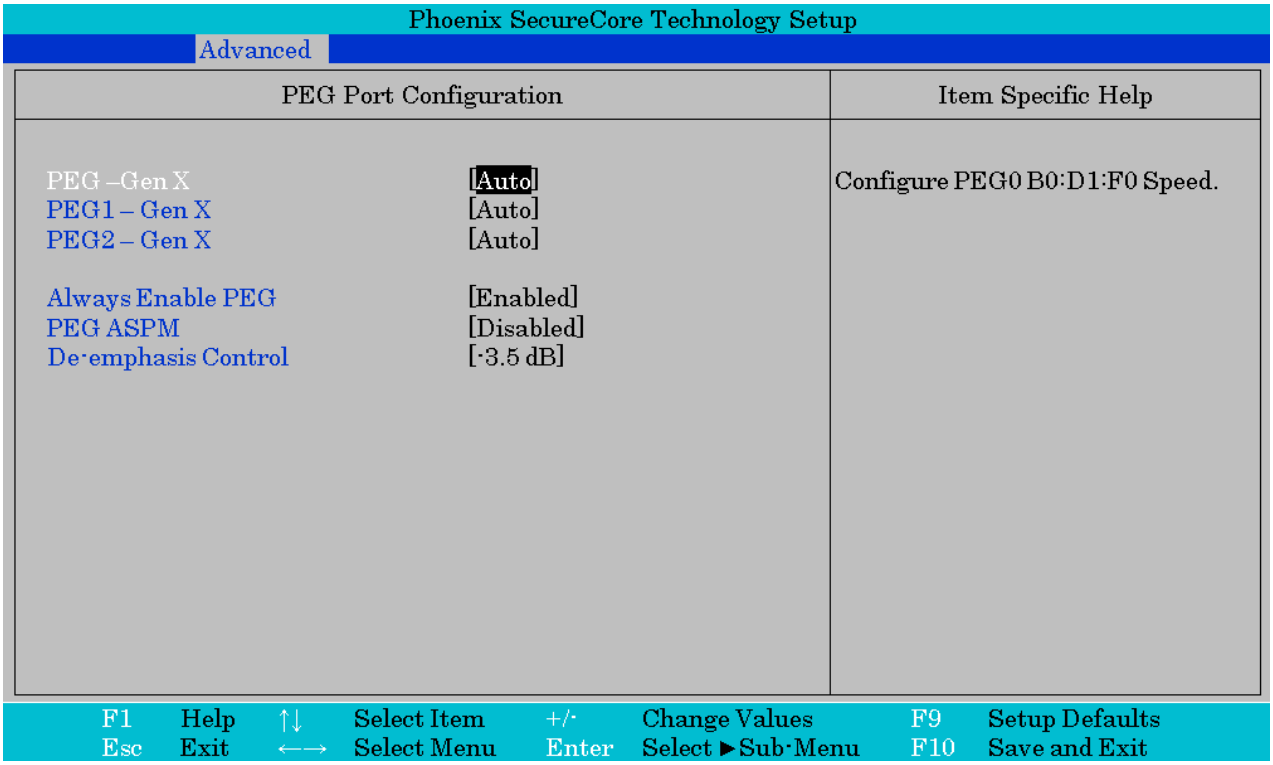
Note 1, only when Switch mode = LVDS.

IGD Configuration



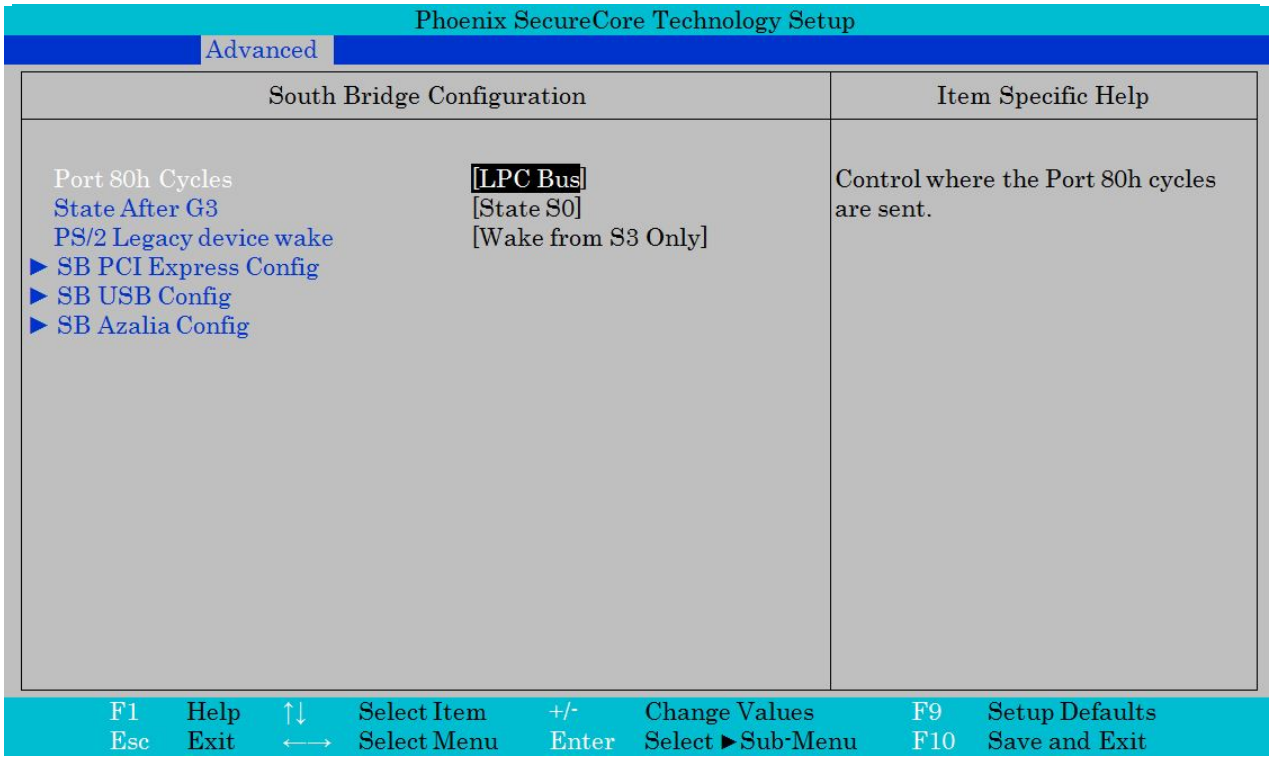
Function	Selection	Description
IGD – Boot Type	**VBIOS Default** EFP EFP3 EFP2	Select the Video Device activated during POST. This has no effect if external graphics are present.

PEG Port Configuration



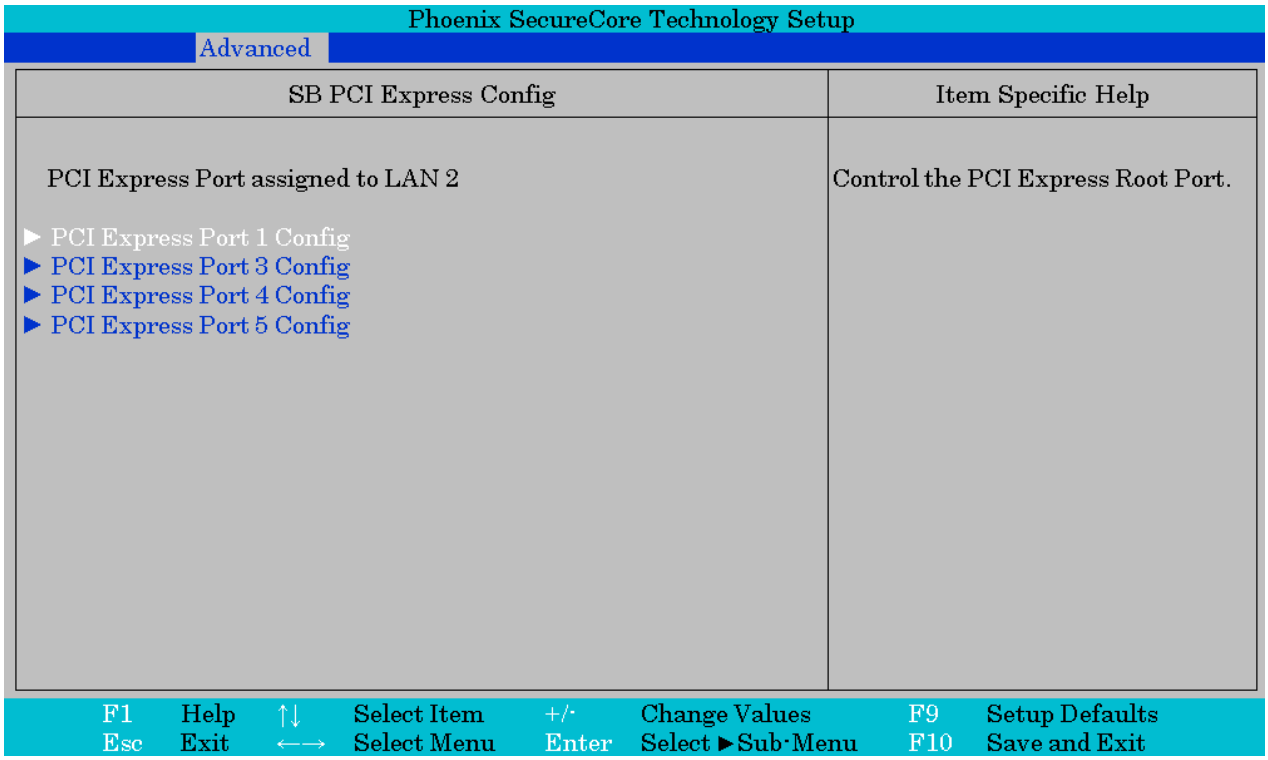
Function	Selection	Description
PEG –Gen X	**Auto** Gen1 Gen2 Gen3	Configure PEG0 B0:D1:F0 Speed.
PEG1 – Gen X	**Auto** Gen1 Gen2 Gen3	Configure PEG1 B0:D1:F1 Speed.
PEG2 – Gen X	**Auto** Gen1 Gen2 Gen3	Configure PEG2 B0:D1:F2 Speed.
Always Enable PEG	Disabled **Enabled**	Enable PEG.
PEG ASPM	**Disabled** L0S L1 L0S And L1 Auto	PEG ASPM Settings.
De-emphasis Control	-6 dB **-3.5 dB**	DeEmphasis control for PEG

South Bridge Configuration

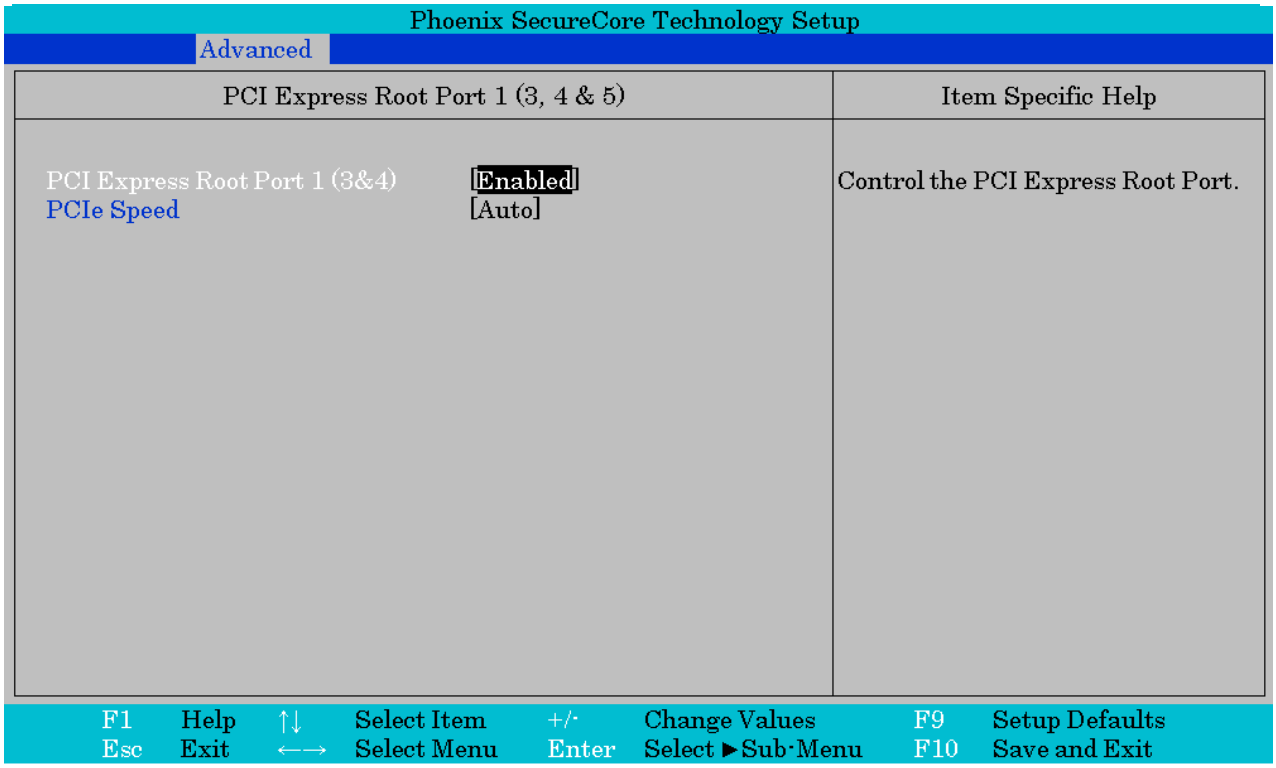


Function	Selection	Description
Port 80h Cycles	**LPC Bus** PCI Bus	Control where the Port 80h cycles are sent.
State After G3	State S5 **State S0**	Specify what state to switch to when power is re-applied after a power failure (G3 state).
PS/2 Legacy device wake	Disabled Wake from S3 Only Wake from S4 Only Wake from S3 and S4 Wake from S5 Only Wake from S3, S4 and S5	Allow wake and/or power-on with PS/2 keyboard or mouse.

SB PCI Express Config

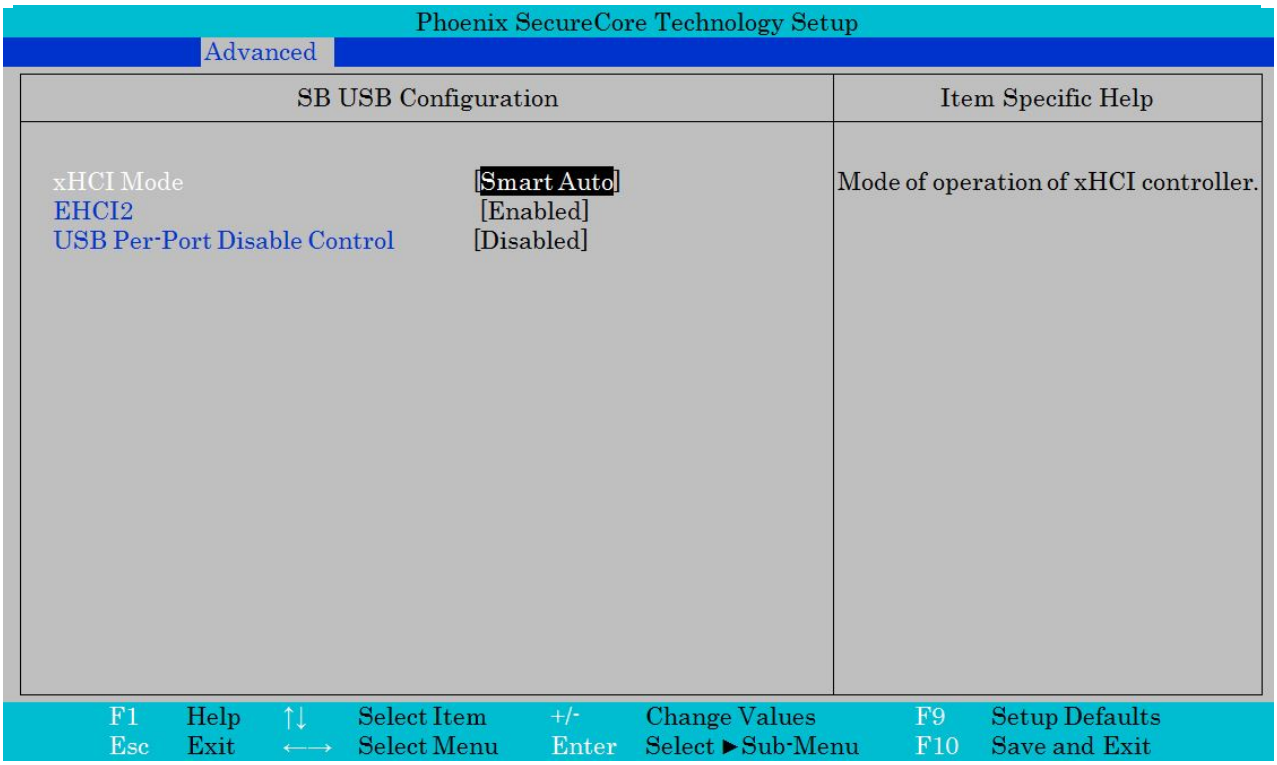


PCI Express Root Port 1 (3, 4 & 5)



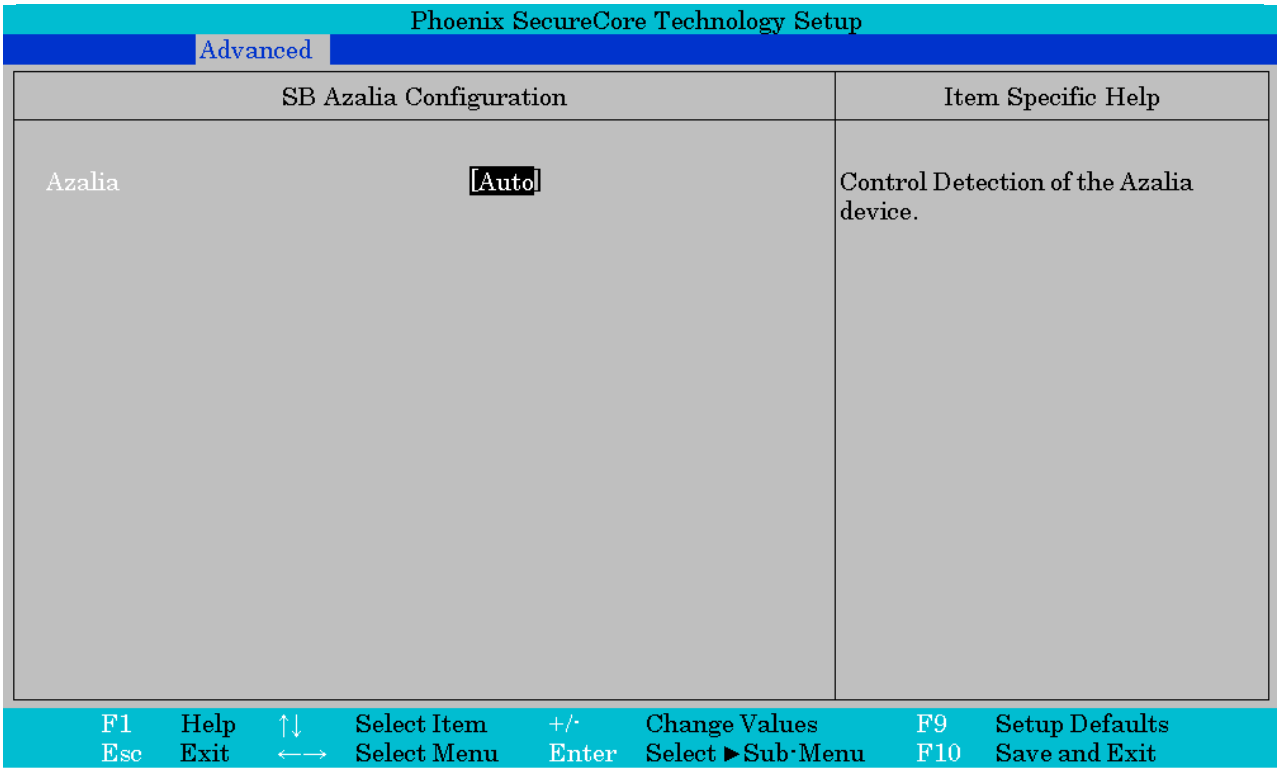
Function	Selection	Description
PCI Express Root Port x (x= 1, 3,4 or 5)	Disabled **Enabled**	Control the PCI Express Root Port.
PCIe Speed	**Auto** Gen1 Gen2	Select PCIe Speed to Gen1 or Gen2.

SB USB Configuration



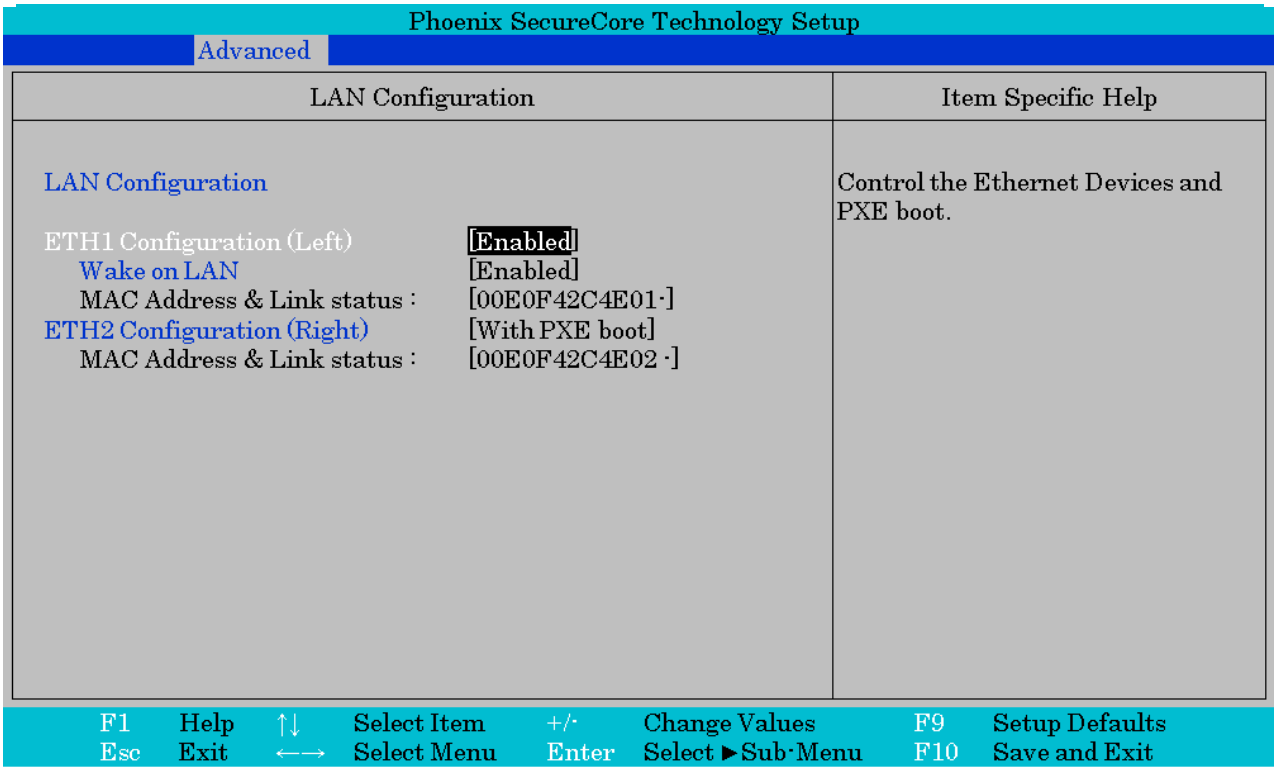
Function	Selection	Description
xHCI Mode	Disabled Enabled Auto **Smart Auto**	Mode of operation of xHCI controller.
EHCI2	Disabled **Enabled**	Control the USB EHCI (USB 2.0) functions.
USB Per-Port Disable Control	**Disabled** Enabled	Control each of the USB ports (0~13) enable/disable.

SB Azalia Configuration



Function	Selection	Description
Azalia	Disabled Enabled **Auto**	Control Detection of the Azalia device.

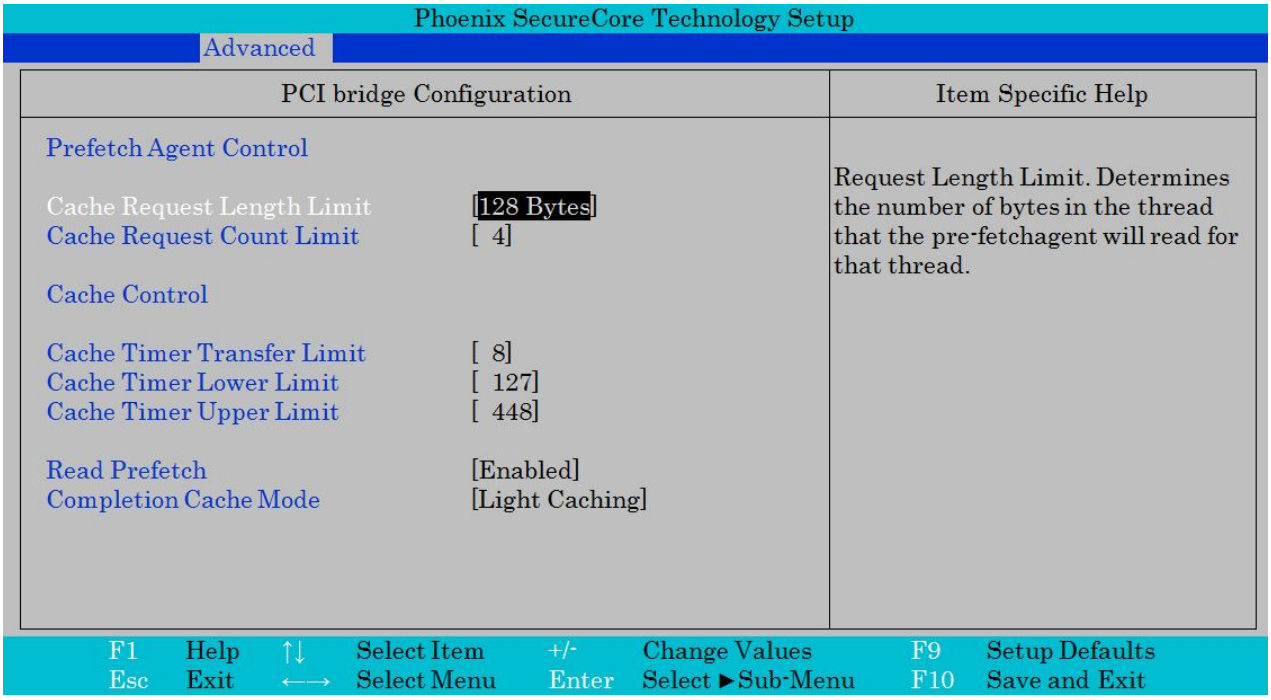
LAN Configuration



Note: The "+" and "-" (to the right of the MAC address) indicates respectively if link is established or not.

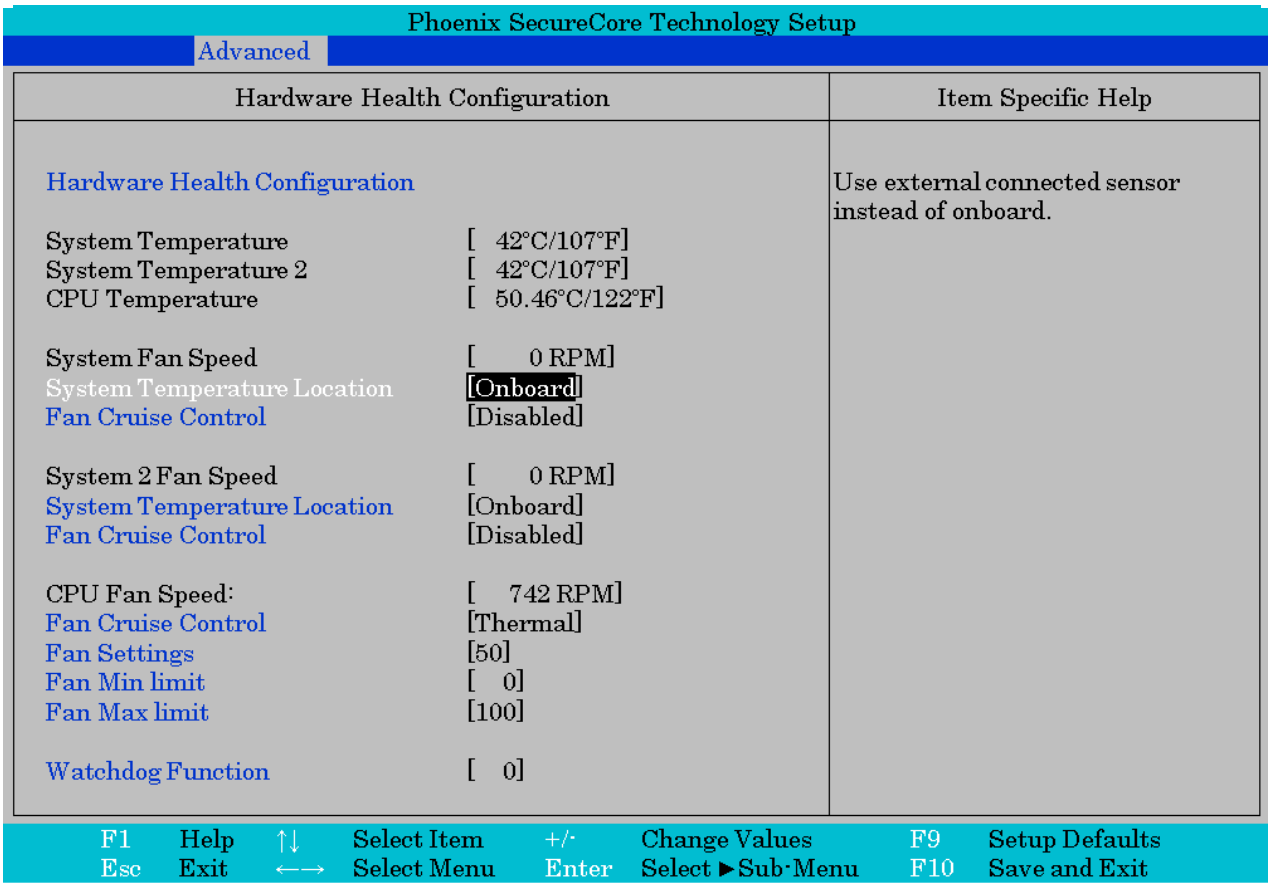
Function	Selection	Description
ETH1 Configuration (Left)	Disabled **Enabled** With PXE boot	Control the Ethernet Devices and PXE boot.
Wake on LAN	Disabled **Enabled**	Enable or disable integrated LAN to wake the system. (The Wake On LAN cannot be disabled if ME is on at Sx state).
ETH2 Configuration (Right)	Disabled **Enabled** With PXE boot	Control the Ethernet Devices and PXE boot.

PCI bridge Configuration



Function	Selection	Description
Cache Request Length Limit	64 Bytes **128 Bytes** 256 Bytes 512 Bytes 1Kbytes 2Kbytes 4Kbytes 8Kbytes	Request Length Limit. Determines the number of bytes in the thread that the pre-fetchagent will read for that thread.
Cache Request Count Limit	0, 1, … 3, **4**, 5, …, 15	Set the number of PCI cycle starts that have to occur without a read hit on the completion data buffer, before the cache data can be discarded.
Cache Timer Transfer Limit	0, 1, … 7, **8**, 9, …, 15	Number of PCI cycle starts that have to occur without a read hit on the completion data buffer, before the cache data can be discarded.
Cache Timer Lower Limit	0, 1,… **127**, … 4096	Minimum number of clock cycles that must have passed without a read hit on the completion data buffer, before the 'cache miss limit' check can be triggered.
Cache Timer Upper Limit	0, 1,… **448**, … 4096	Discard cache data after this number of clock cycles have passed without a read hit on the completion data buffer.
Read Prefetch	**Enabled** Disabled	Control the pre-fetch functionality on PCI memory read transactions.
Completion Cache Mode	No Caching **Light Caching** Full Caching	Determines the rules for completing the caching process. Light caching: All remaining read completion data will be discarded after any of the data has been returned to the PCI master. Light & Full caching: Pre-fetching is enabled. All remaining read completion data will be cached after data has been returned to the PCI master and the PCI master terminated the transfer with RETRY. Full caching: All remaining read completion data will be cached after data has been returned to the PCI master and the PCI master terminated the transfer.

Hardware Health Configuration



Note: *System Temperature* readout is the temperature measured by the selected sensor via *System Temperature Location*. Example, if using same *System Temperature Location* selection for both *System Fan* and *System 2 Fan* then *System Temperature* and *System Temperature2* readout will be identical.

Function	Selection	Description
System Temperature Location	**Onboard** LM75 @ 0x90 (Note 1)	Use external connected sensor instead of onboard.
Fan Cruise Control (Note 2)	Disabled Thermal Speed	Disabled = Full speed. Thermal: Regulate according to specified °C. Speed: Regulate according to specified RPM.
Fan Settings	30 – 90 (note3) 1000 – 10000 (note4)	
Fan Min limit (Note 5)	0 (note6)	Minimum PWM %, can be used to make sure fan is always active. Make sure Min limit < Max limit.
Fan Max limit (Note 5)	100 (note6)	Maximum PWM %, can be used to limit the fan noise. Make sure Min limit < Max limit.
Watchdog Function	0 - 255 (note7)	0 = Disabled. Enter the service interval in seconds before system will reset.

Note 1: When selecting LM75 @ 0x90 then the *System Temperature* and/or *System Temperature 2* readout will only be valid if the sensor is physically connected to the Feature connector.

Note 2: Three sets of settings (*Fan Cruse Control*, *Fan Settings*, *Fan Min limit*, *Fan Max limit*), one set for *System Fan*, one set for *System 2 Fan* and one set for *CPU Fan*. The *Fan Cruise Control* is by default *Disabled* for *System Fan* and *System 2 Fan* and by default *Thermal* for CPU Fan.

Note 3: °C (if *Fan Cruise Control* is *Thermal*) use either digit keys to enter value or +/- keys to increase/decrease value. Don't use mix of digit keys and +/- keys.

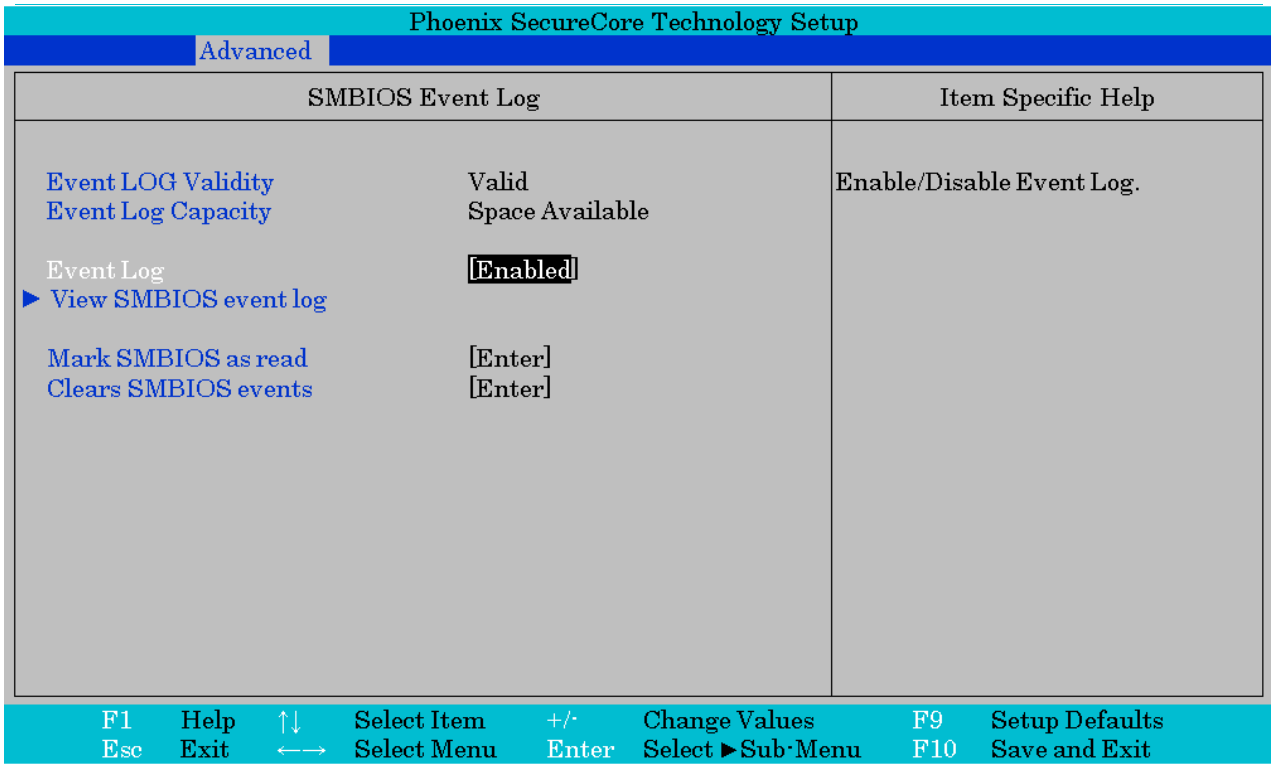
Note 4: RPM (if *Fan Cruise Control* is *Speed*) use either digit keys to enter value or +/- keys to increase/decrease value by 100. Don't use mix of digit keys and +/- keys.

Note 5: Only visible if *Fan Cruise Control* is *Thermal*.

Note6: Use number keys to enter value.

Note 7: Seconds, use digit keys to enter value. Value 0 means Watchdog is disabled. Refer to "KT-API-V2 User Manual" to control the Watchdog via API or refer to "KT-API-V2 User Manual DLL" how to control Watchdog via Windows DLL.

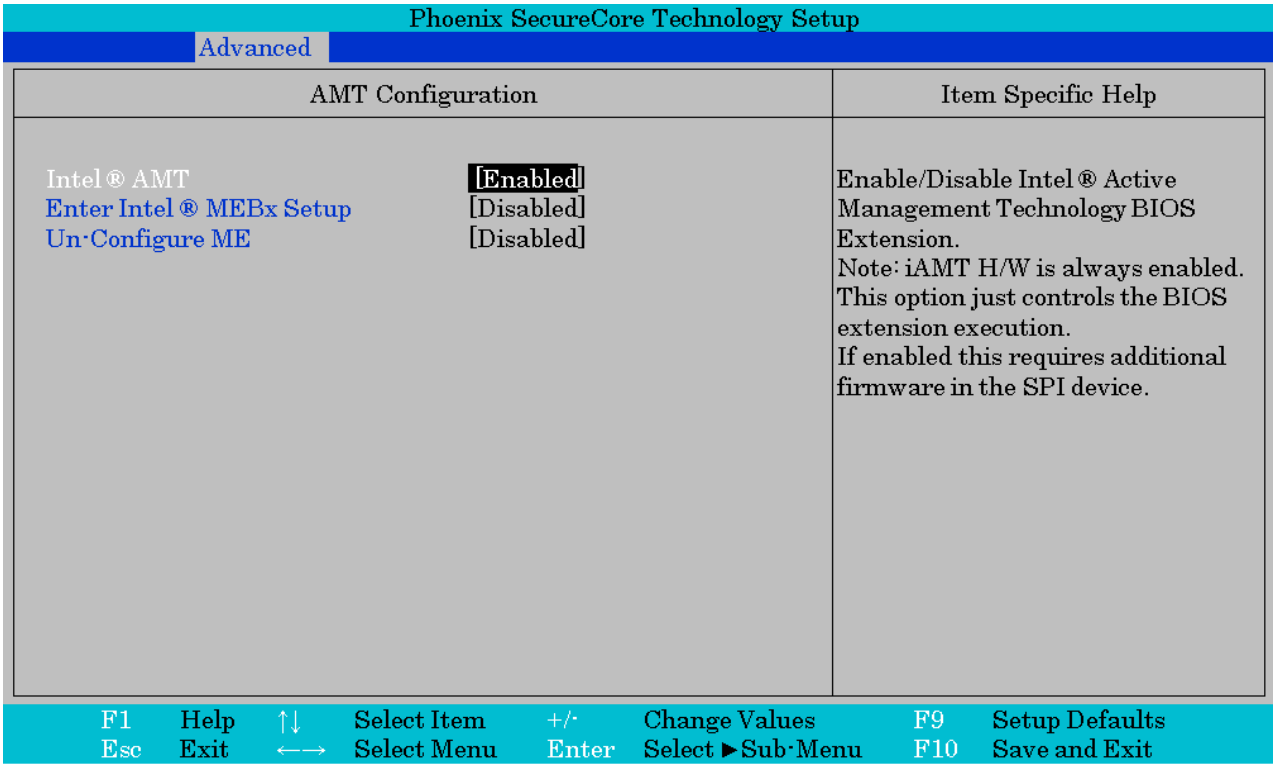
SMBIOS Event Log



Note: Entering *View SMBIOS event log* will show log only.

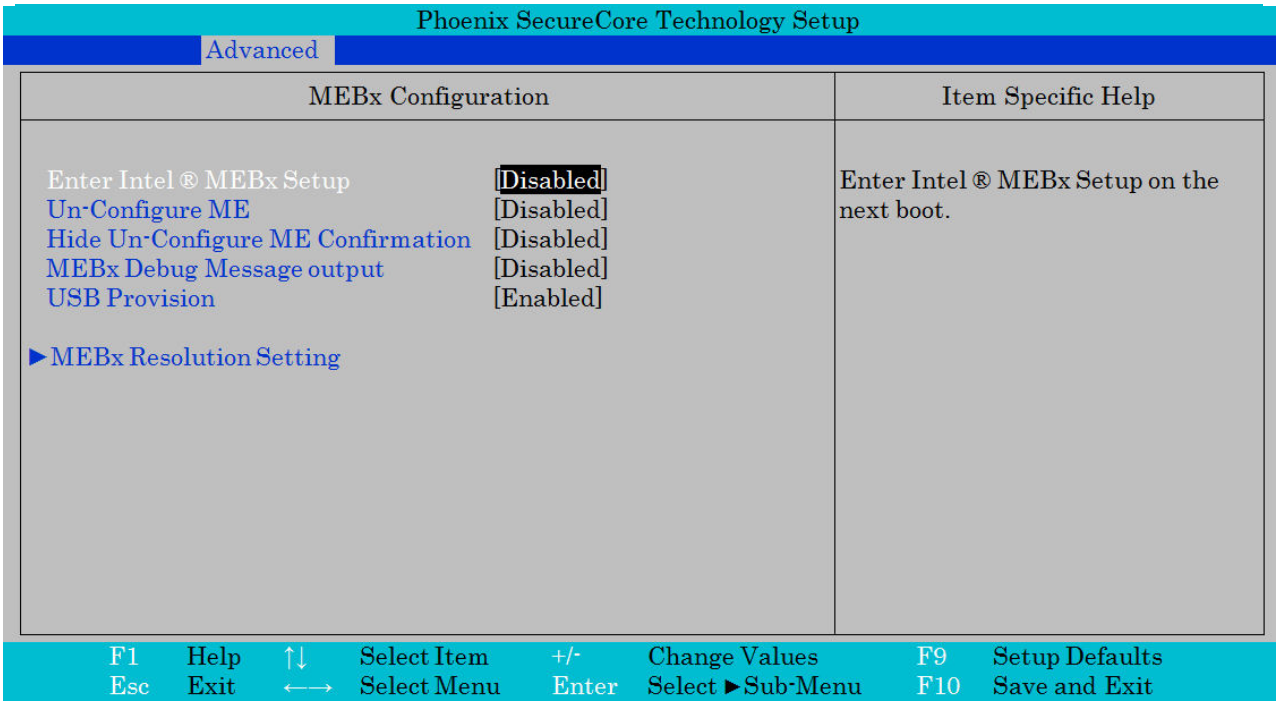
Function	Selection	Description
Event Log	Disabled **Enabled**	Enable/Disable Event Log.
Mark SMBIOS as read	Enter	Mark SMBIOS events as read. Marked SMBIOS events won't be displayed.
Clears SMBIOS events	**Enter**	Clears SMBIOS events.

AMT Configuration



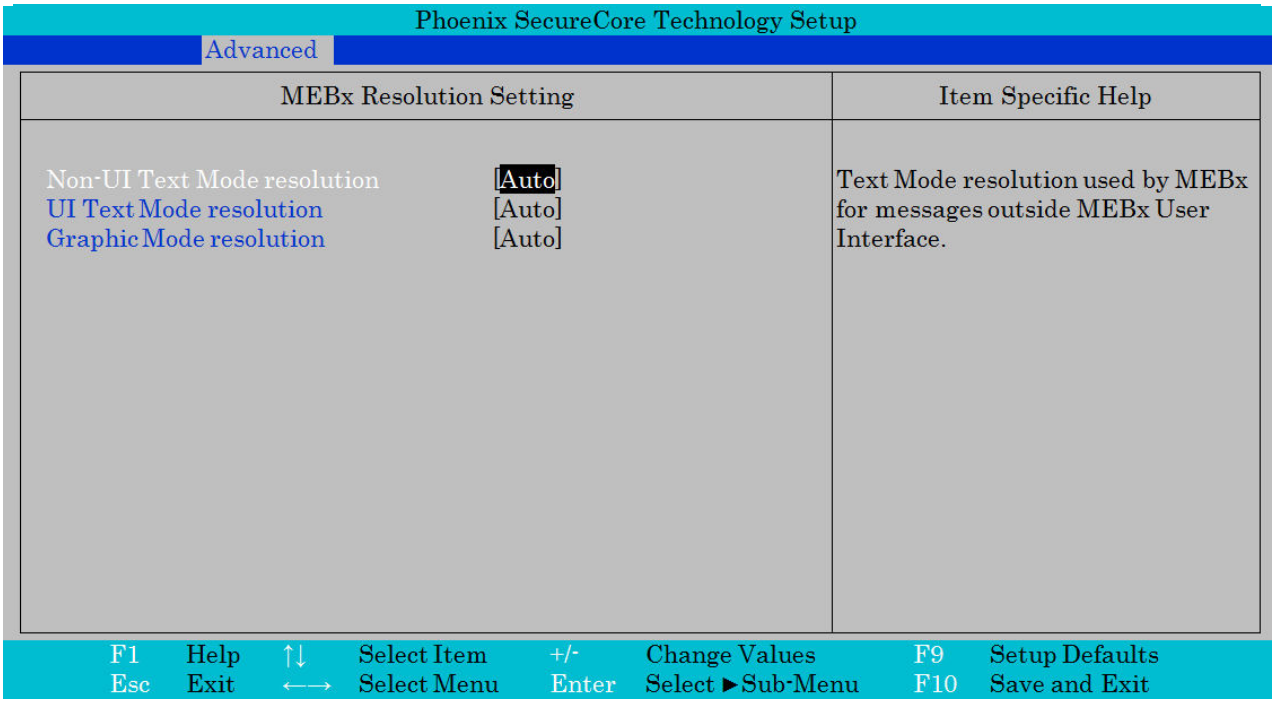
Function	Selection	Description
Intel ® AMT	Disabled **Enabled**	Enable/Disable Intel ® Active Management Technology BIOS Extension. Note: iAMT H/W is always enabled. This option just controls the BIOS extension execution. If enabled this requires additional firmware in the SPI.
Enter Intel ® MEBx Setup	**Disabled** Enabled	Enter Intel ® MEBx Setup on the next boot.
Un-Configure ME	**Disabled** Enabled	Un-configure ME without a password.

MEBx Configuration



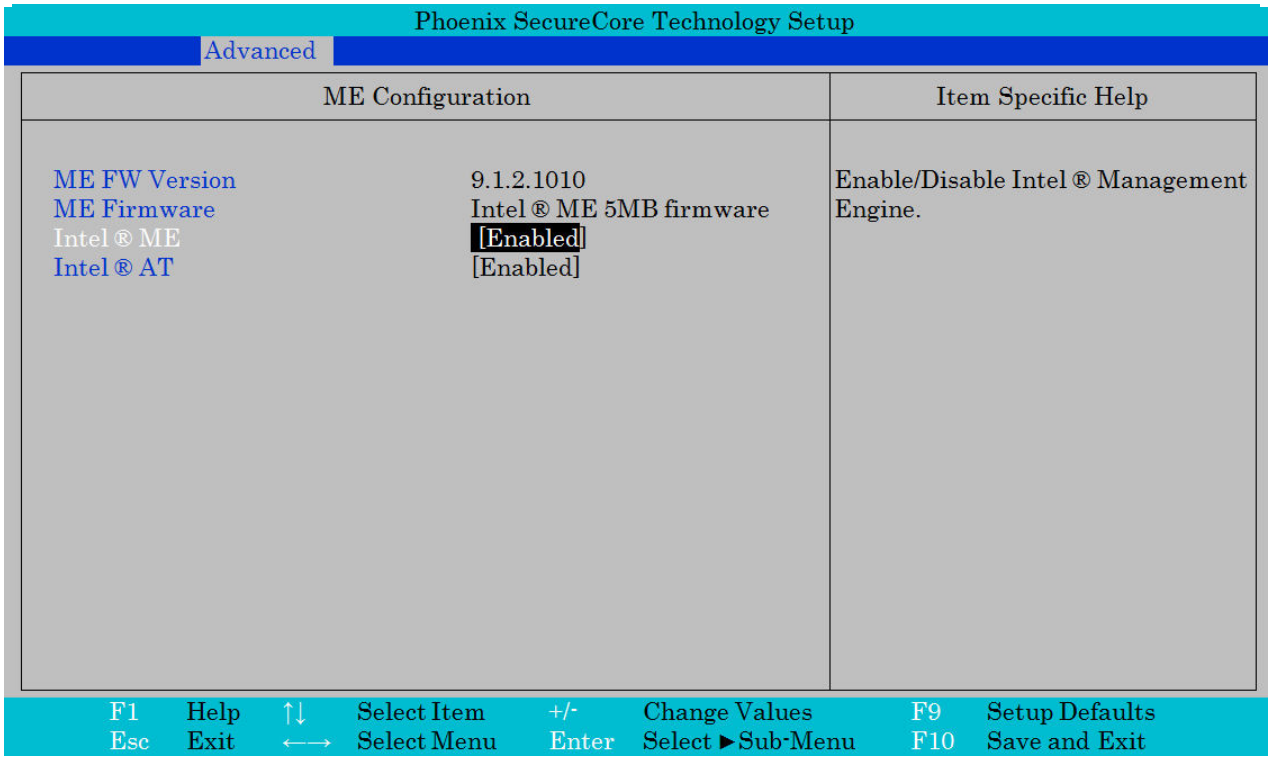
Function	Selection	Description
Enter Intel ® MEBx Setup	**Disabled** Enabled	Enter Intel ® MEBx Setup on the next boot.
Un-Configure ME	**Disabled** Enabled	Un-Configure ME without a password.
Hide Un-Configure ME Confirmation	**Disabled** Enabled	Hide Un-Configure ME Confirmation without password Confirmation Prompt.
MEBx Debug Message output	**Disabled** Enabled	Enable/Disable MEBx Debug Message output.
USB Provision	Disabled **Enabled**	Enable/Disable USB Provision function.

MEBx Resolution Setting



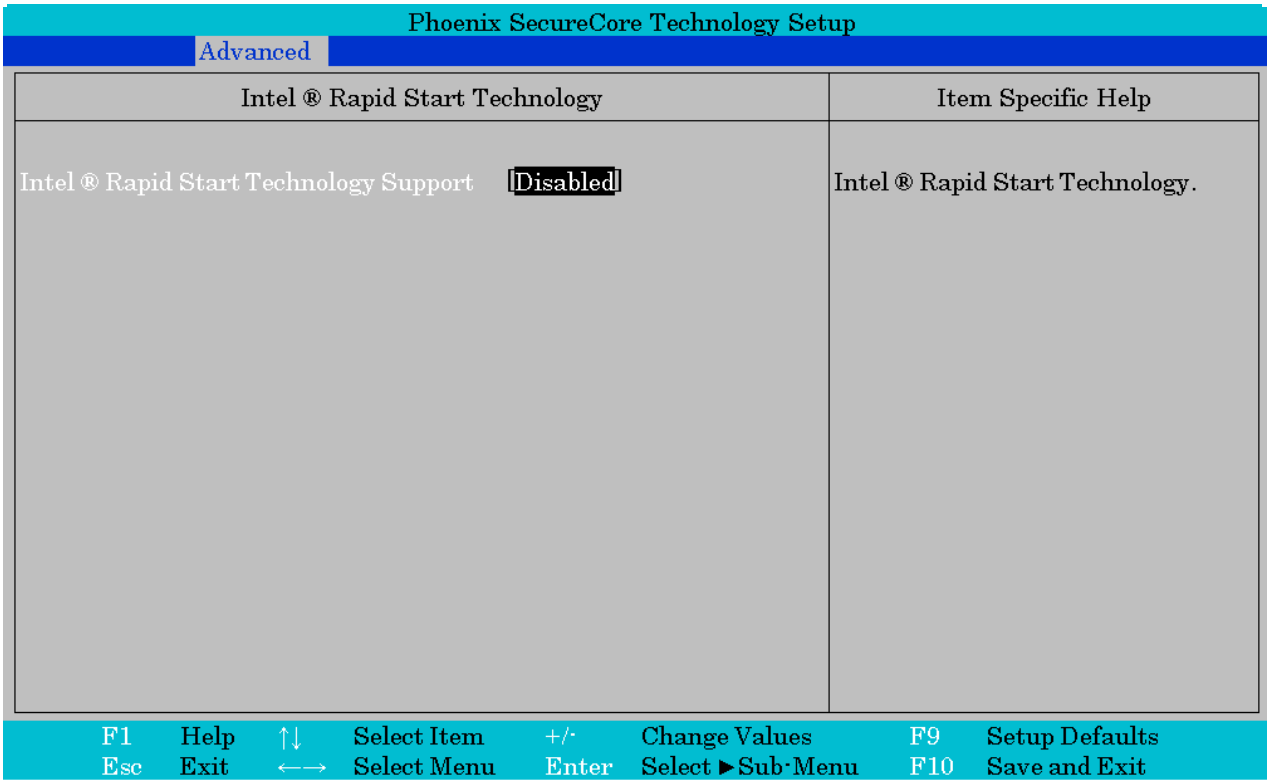
Function	Selection	Description
Non-UI Text Mode resolution	**Auto** 80X25 100X31	Text Mode resolution used by MEBx for messages outside MEBx User Interface.
UI Text Mode resolution	**Auto** 80X25 100X31	Text Mode resolution used by MEBx to display the User Interface forms.
Graphic Mode resolution	**Auto** 640X480 800X600 1024X768	Graphic Mode resolution used by MEBx to display boxes like consent sprite.

ME Configuration



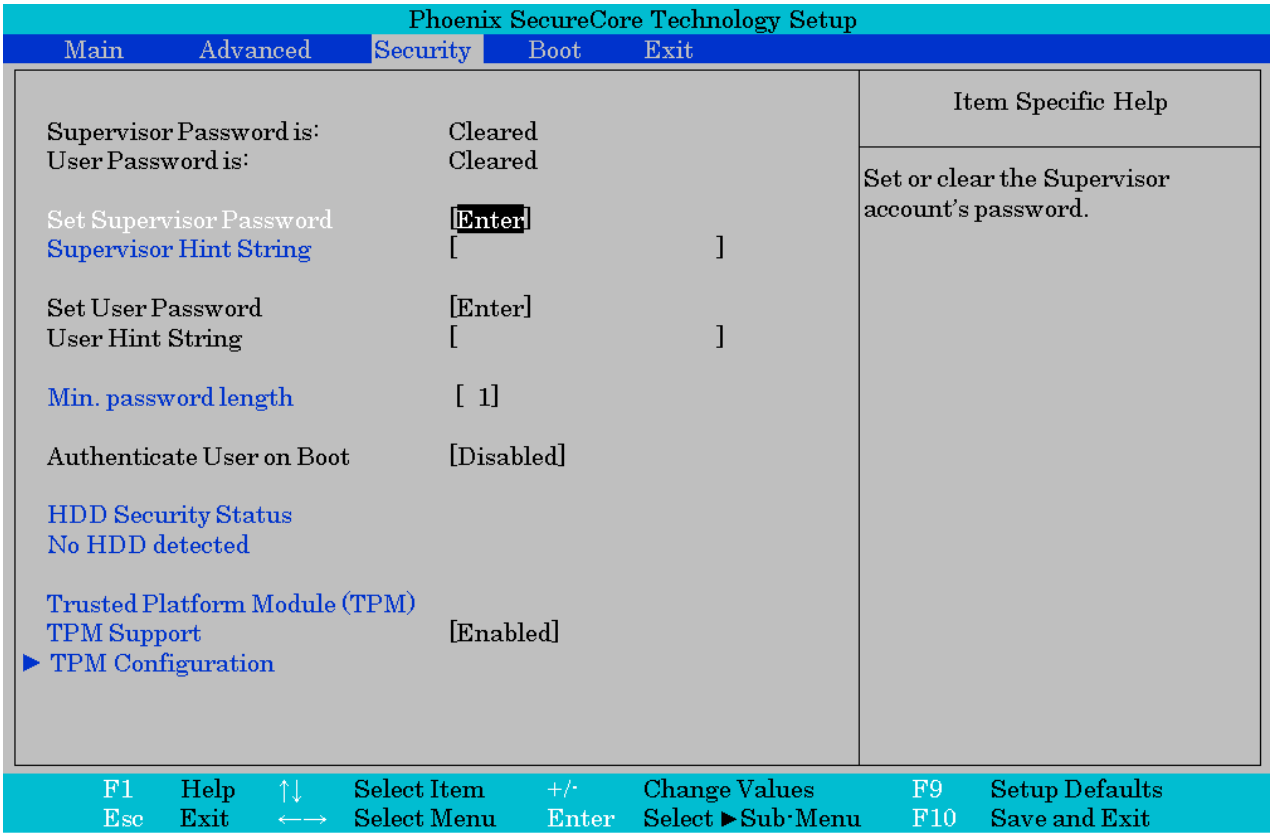
Function	Selection	Description
Intel ® ME	Disabled **Enabled**	Enable/Disable Intel ® Management Engine.
Intel ® AT	Disabled **Enabled**	Enable/Disable Intel ® Anti-Theft Technology.

Intel ® Rapid Start Technology



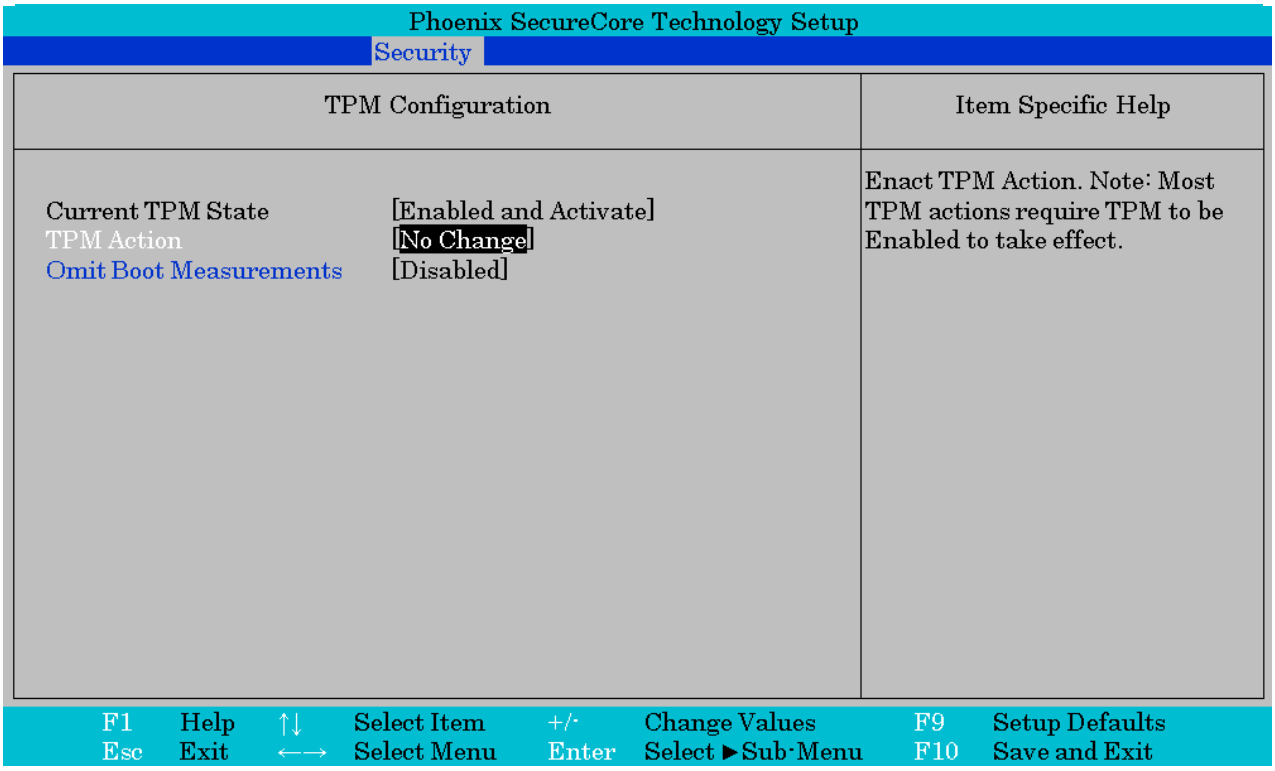
Function	Selection	Description
Intel ® Rapid Start Technology Support	**Disabled** Enabled	Intel ® Rapid Start Technology.

10.3 Security



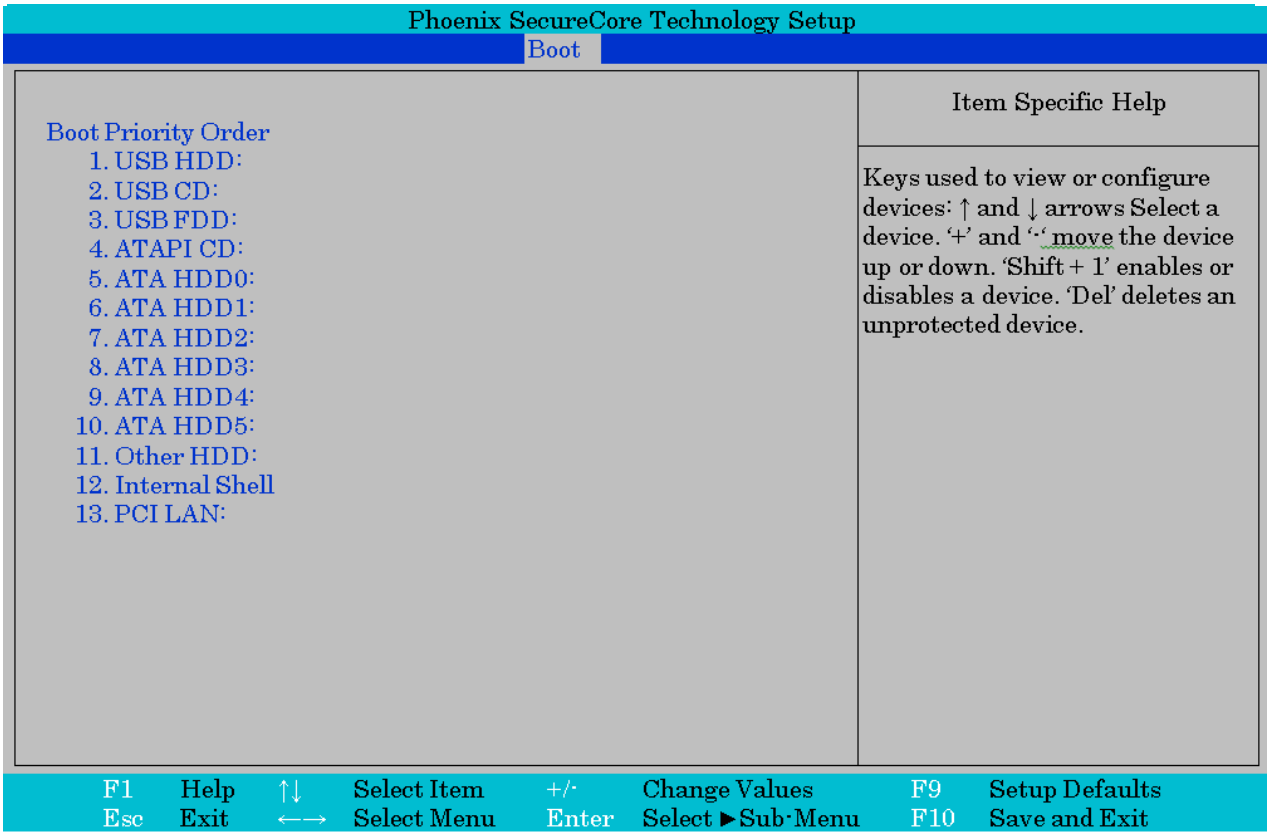
Function	Selection	Description
Set Supervisor Password	(up to 20 characters)	Set or clear the Supervisor account's password.
Supervisor Hint String	(up to 20 characters)	Press Enter to type Supervisor Hint String.
Min. password length	1, 2, ..., 20	Set the minimum number of characters for password (1-20).
TPM Support	Disabled **Enabled**	This is used to decide whether TPM support should be enabled or disabled.

TPM Configuration

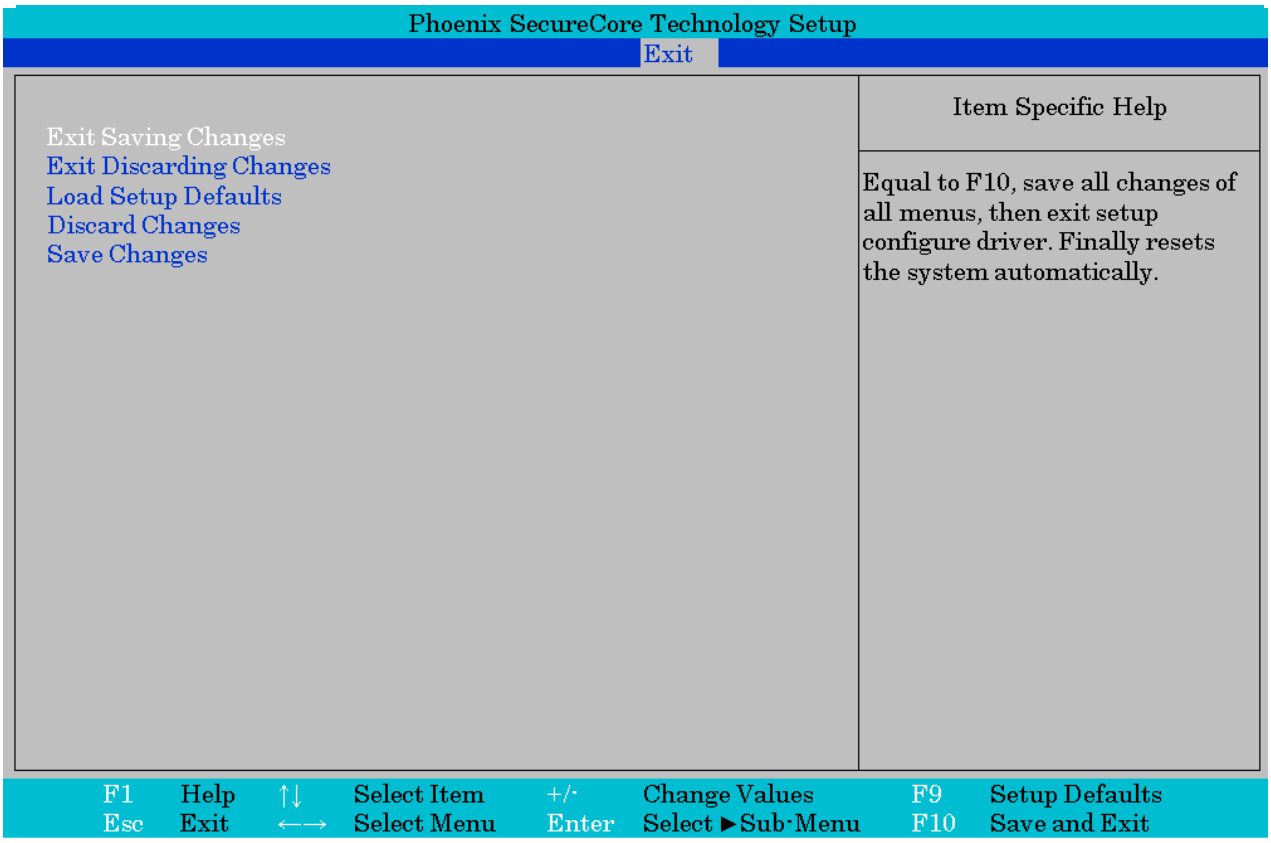


Function	Selection	Description
TPM Action	No Change Enable Disable Activate Deactivate Clear Enable and Activate Disable and Deactivate Set Owner Install, with State=True Set Owner Install, with State=False Enable, Activate, and Set Owner Install, with State=True Disable, Deactivate, and Set Owner Install, with State=False Clear, Enable, and Activate Require PP for provisioning Do not require PP for provisioning Require PP for clear Do not require PP for clear Enable, Activate, and Clear Enable, Activate, Clear, Enable, and Activate	Enact TPM Action. Note: Most TPM actions require TPM to be Enabled to take effect.
TPM Support	**Disabled** Enabled	Enabling this option causes the system to omit recording boot device attempts in PCR[4].

10.4 Boot


Phoenix SecureCore Technology Setup
Boot
Item Specific Help
Boot Priority Order
1. USB HDD:
2. USB CD:
3. USB FDD:
4. ATAPI CD:
5. ATA HDD0:
6. ATA HDD1:
7. ATA HDD2:
8. ATA HDD3:
9. ATA HDD4:
10. ATA HDD5:
11. Other HDD:
12. Internal Shell
13. PCI LAN:
Keys used to view or configure devices: ↑ and ↓ arrows Select a device. '+' and '-' move the device up or down. 'Shift + 1' enables or disables a device. 'Del' deletes an unprotected device.
F1 Help ↑↓ Select Item +/- Change Values F9 Setup Defaults
Esc Exit ←→ Select Menu Enter Select ▶Sub-Menu F10 Save and Exit

10.5 Exit



Function	Description
Exit Saving Changes	Equal to F10, save all changes of all menus, then exit setup configure driver. Finally resets the system automatically.
Exit Discarding Changes	Equal to ESC, never save changes, then exit setup configure driver.
Load Setup Defaults	Equal to F9. Load standard defaults values.
Discard Changes	Load the original value of this boot time. Not the default Setup value.
Save Changes	Save all changes of all menus, but do not reset system.